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ATX

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RLK Platform

CPU:

Rocket lake S

System Chipset:

Z590 PCH_H

Onboard Chip:

SIO:NTC6687

LAN-Intel I225

Flash ROM: SPI 256 MB X1

HD Audio Codec:ALC897

Main Memory:

*DDRIV (5000MHz) * 4 (Dual Channel)*

ACPI:

LDO

PWM:

IMVP8 -RT3609

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X4) Slot * 1*

*PCI Express (X1) Slot * 2*

*M2 (X4) Slot * 3*

Other:

*SATA3.0 *6*

*USB2.0 *8*

*REAL USB3.0 *2+TYPEC*1*

*FRONT USB3.0 *4+TYPEC*1*

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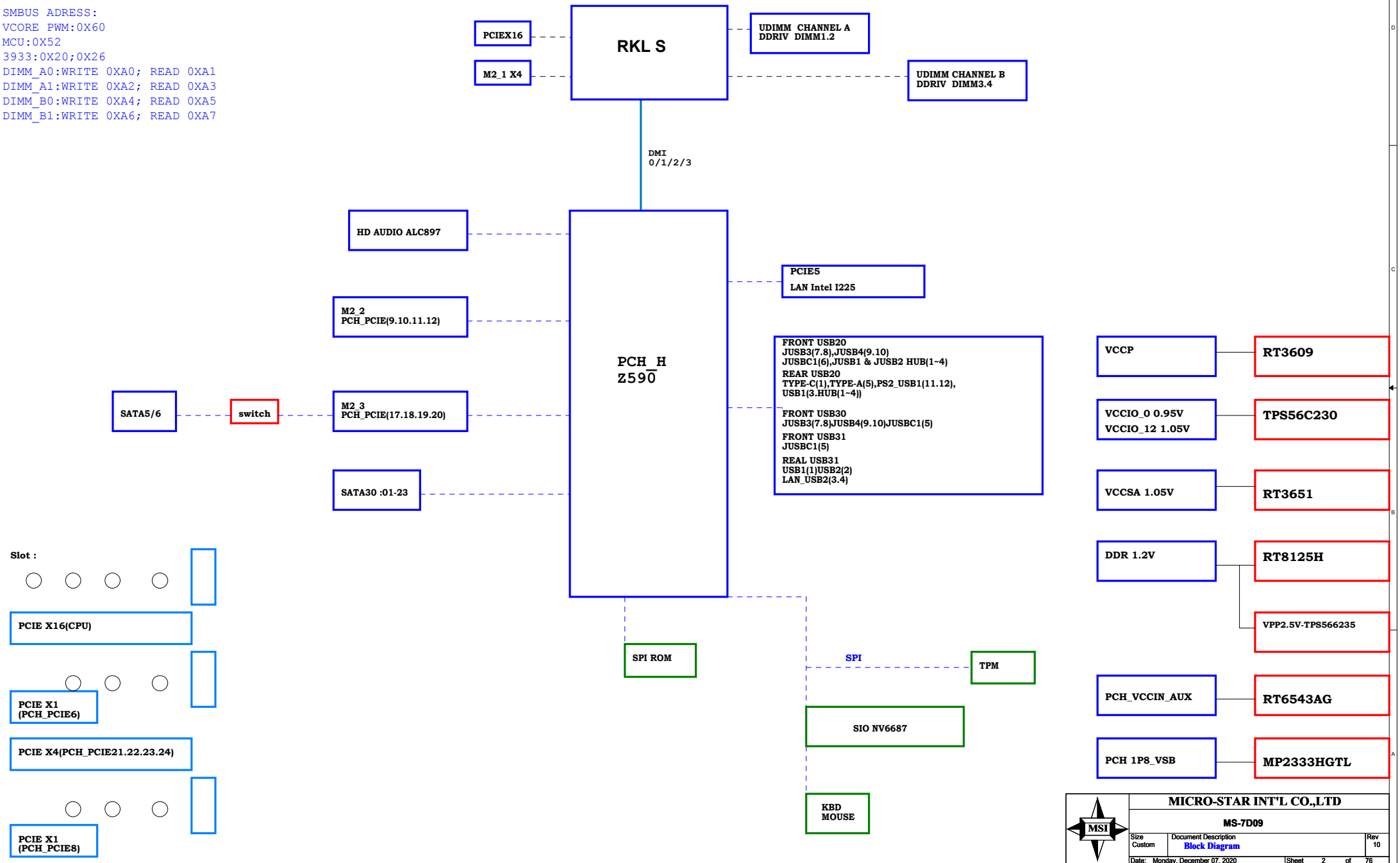
Block Diagram

SMBUS ADRESS:
VCORE PWM:0X60
MCU:0X52
3933:0X20;0X26
DIMM_A0:WRITE 0XA0; READ 0XA1
DIMM_A1:WRITE 0XA2; READ 0XA3
DIMM_B0:WRITE 0XA4; READ 0XA5
DIMM_B1:WRITE 0XA6; READ 0XA7



MSI	MICRO-STAR INT'L CO.,LTD	
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Size Custom	Document Description Block Diagram	Rev 10
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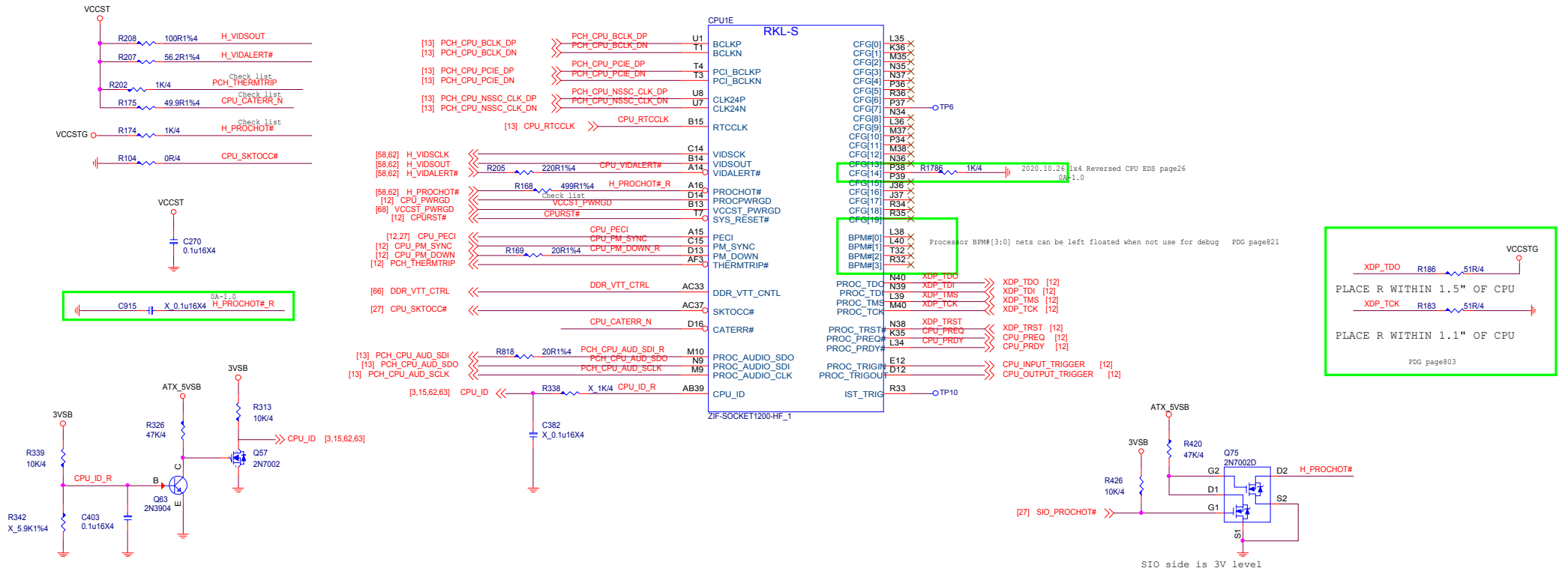

X8 and X4 Ctrl

CFG5 CFG6

ENABLE#		SLOT1	SLOT4	SLOT6
X8	X4			
0	0	X8	X4	X4
0	1	X8	X8	X0
1	0	None	None	None
1	1	X16	X0	X0

CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	1x4	1x4 Reversed	1K Pu down
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

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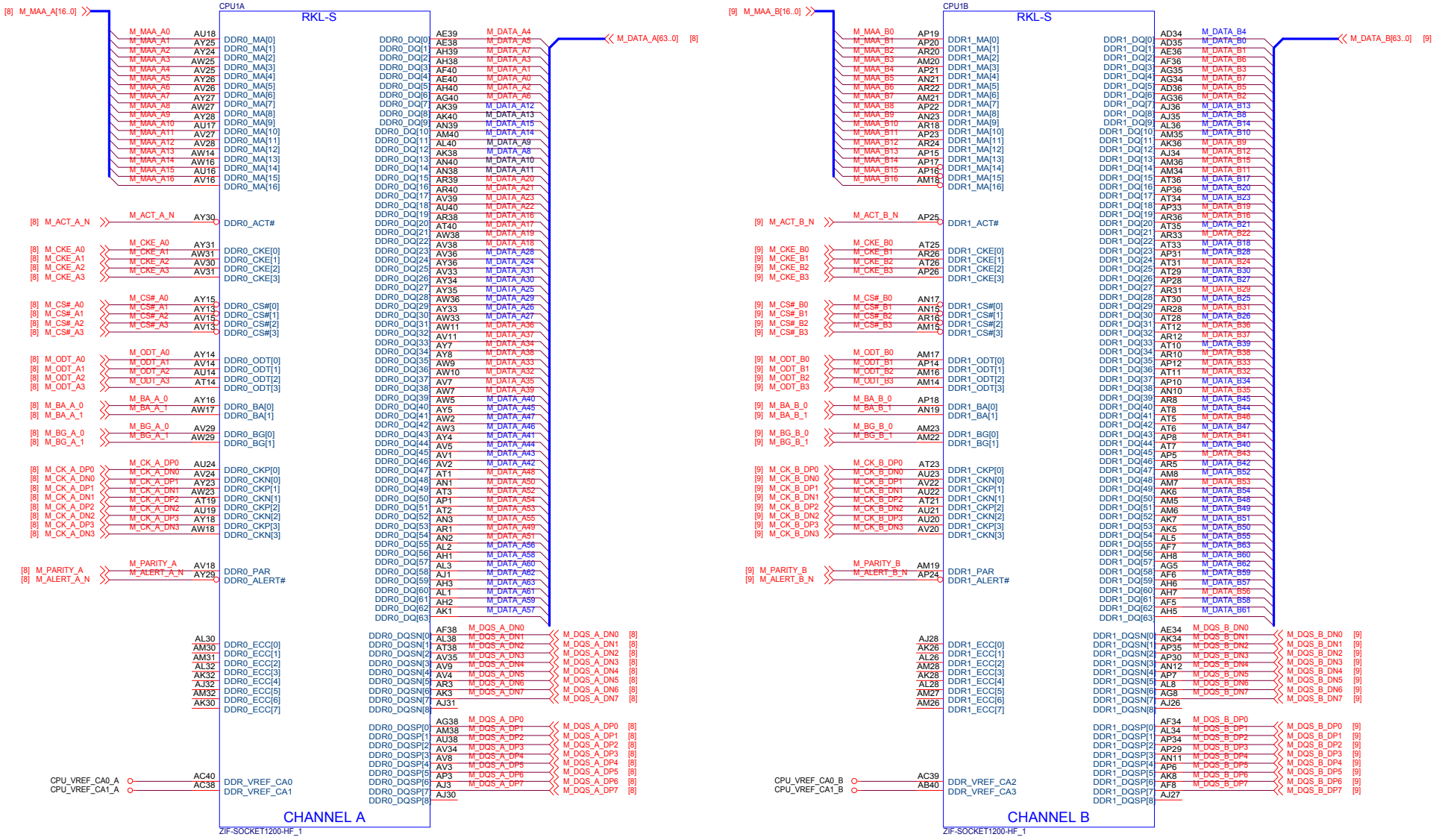

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Size	Document Description	Rev
Custom	CPU-Memory	10

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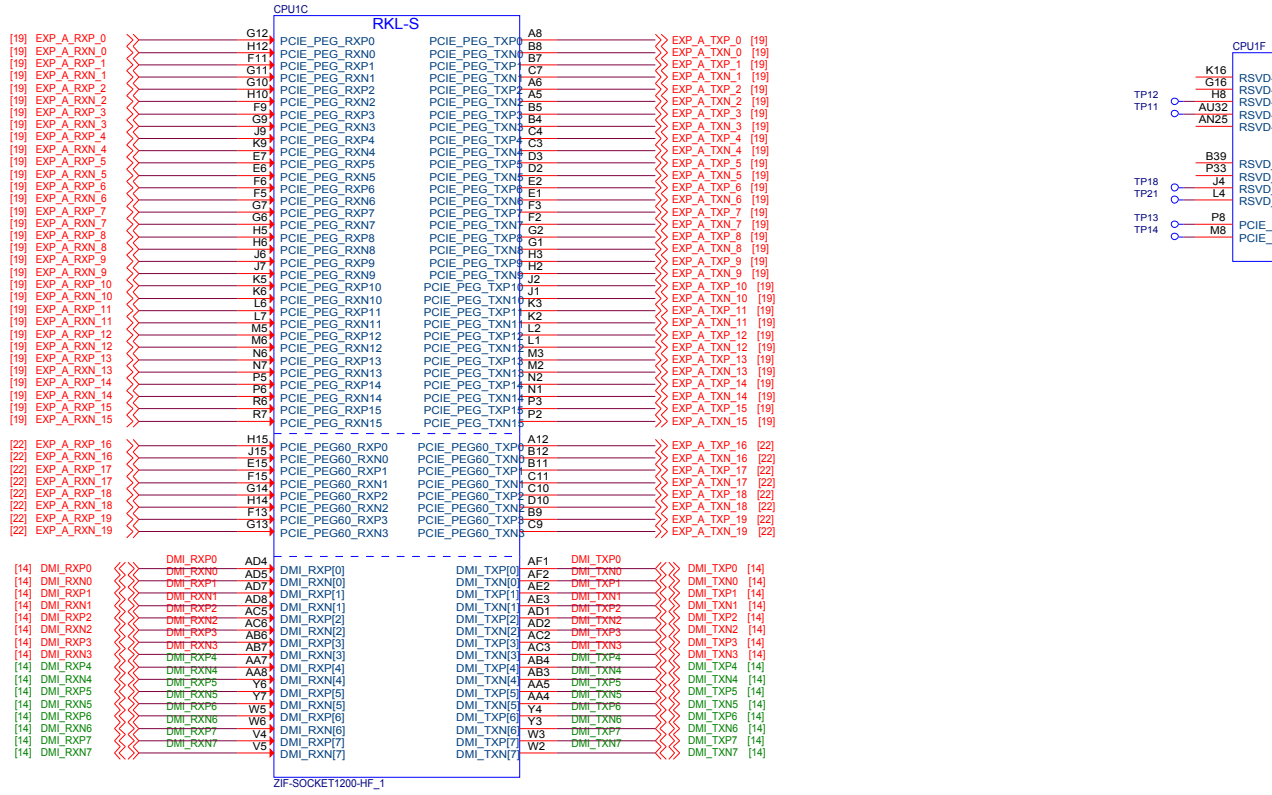

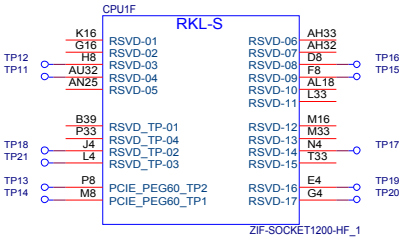

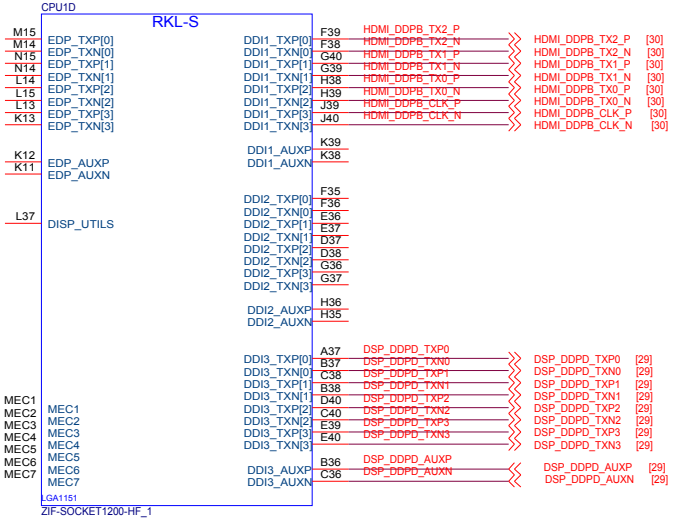

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D09	
Size: Custom	Document Description: CPU-PEG/Display/RSD	Rev: 10
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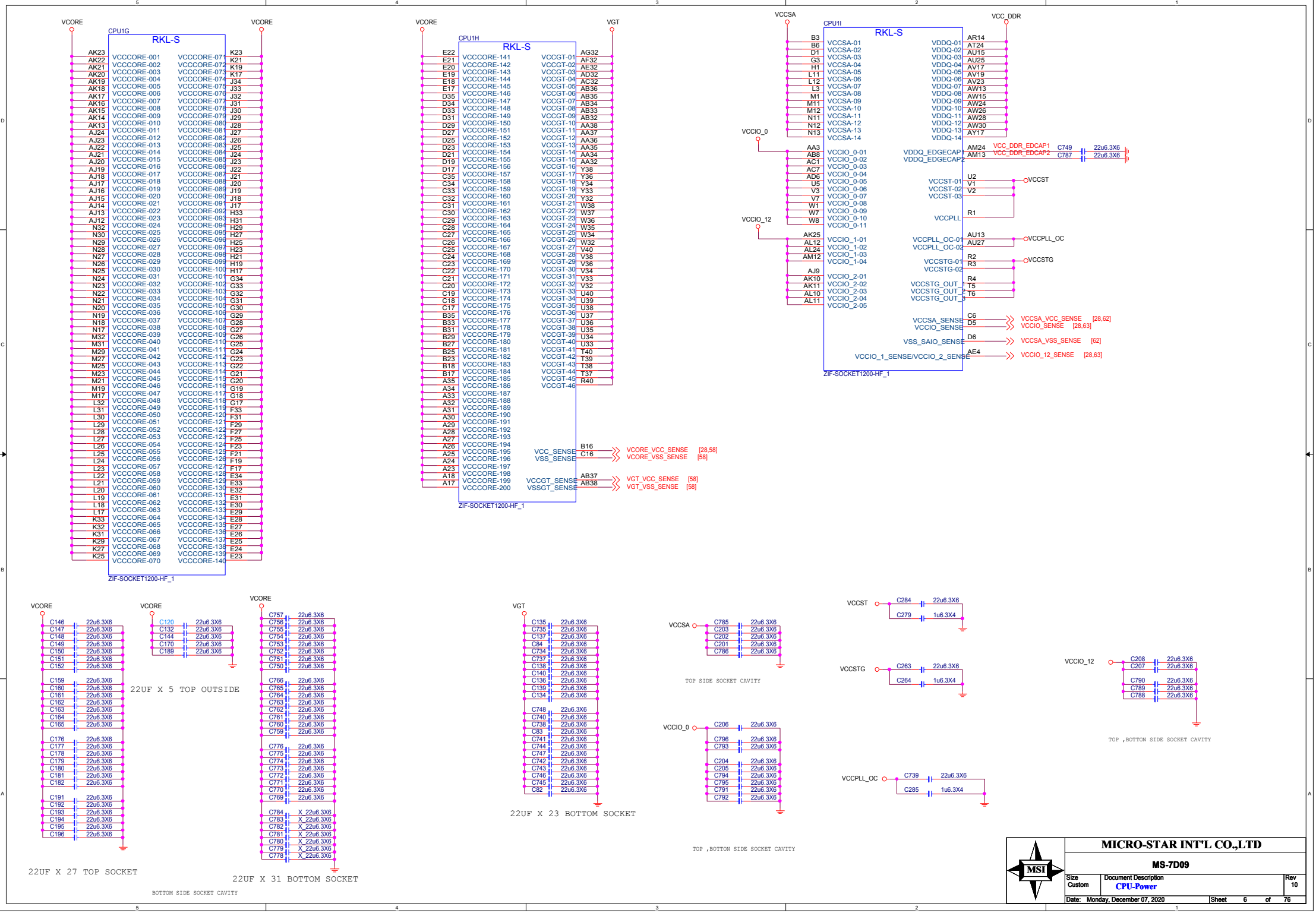
CPU1G
RKL-S
VCORE
ZIF-SOCKET1200-HF_1
CPU1H
RKL-S
VCORE
VGT
VCC_SENSE
VSS_SENSE
VCORE_VCC_SENSE [28,58]
VCORE_VSS_SENSE [58]
VCCGT_SENSE
VSSGT_SENSE
VGT_VCC_SENSE [58]
VGT_VSS_SENSE [58]
CPU1I
RKL-S
VCCSA
VCC_DDR
VCCIO_0
VCCIO_12
VDDQ_EDGECAP1
VDDQ_EDGECAP2
VCC_DDR_EDCAP1
VCC_DDR_EDCAP2
VCCST
VCCPLL
VCCPLL_OC
VCCSTG
VCCSA_SENSE
VCCIO_SENSE
VCCSA_VCC_SENSE [28,62]
VCCIO_SENSE [28,63]
VSS_SAIO_SENSE
VCCSA_VSS_SENSE [62]
VCCIO_1_SENSE/VCCIO_2_SENSE
VCCIO_12_SENSE [28,63]
22UF X 5 TOP OUTSIDE
22UF X 27 TOP SOCKET
22UF X 31 BOTTOM SOCKET
BOTTOM SIDE SOCKET CAVITY
22UF X 23 BOTTOM SOCKET
TOP SIDE SOCKET CAVITY
TOP ,BOTTON SIDE SOCKET CAVITY
TOP ,BOTTON SIDE SOCKET CAVITY
MICRO-STAR INT'L CO.,LTD
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Document Description CPU-Power
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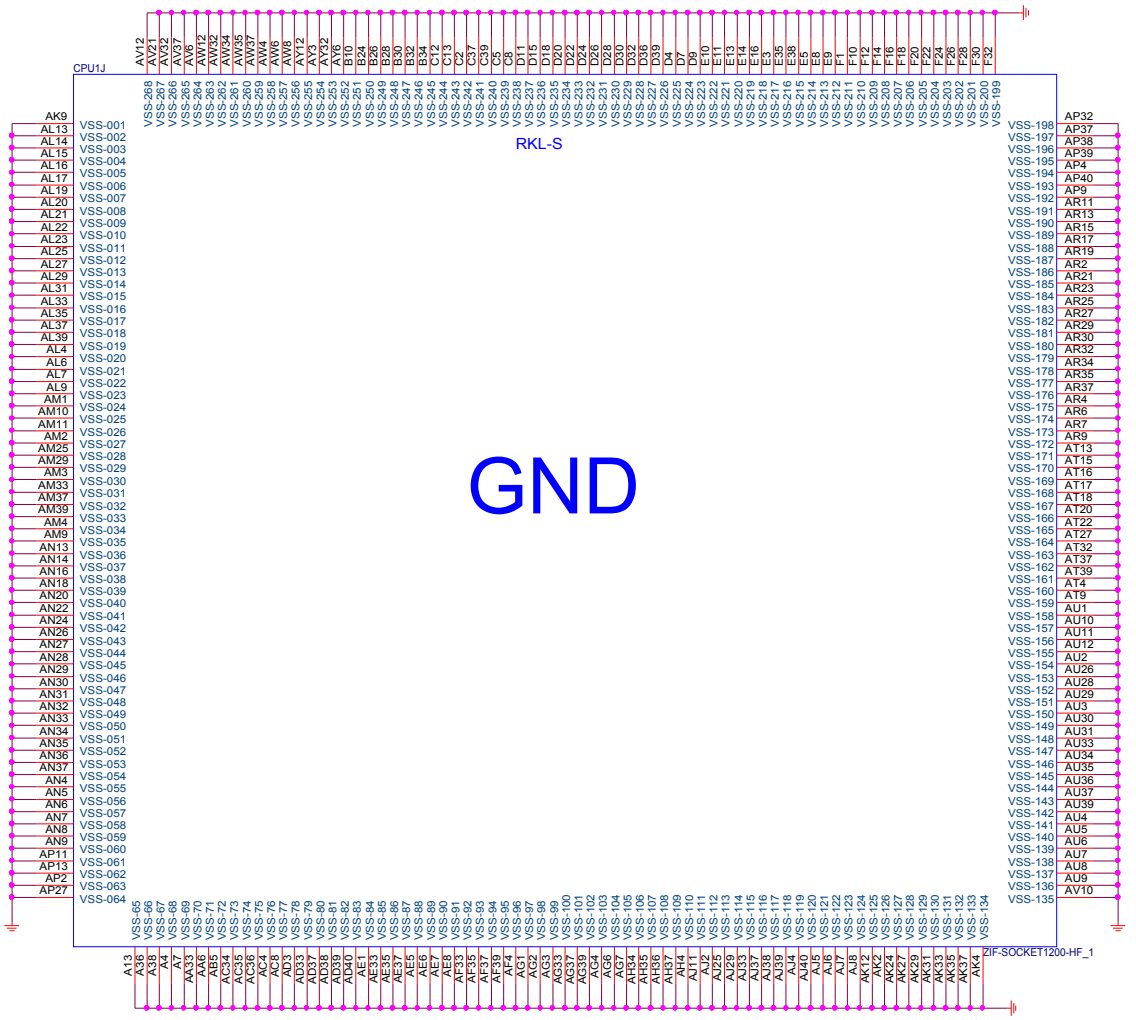

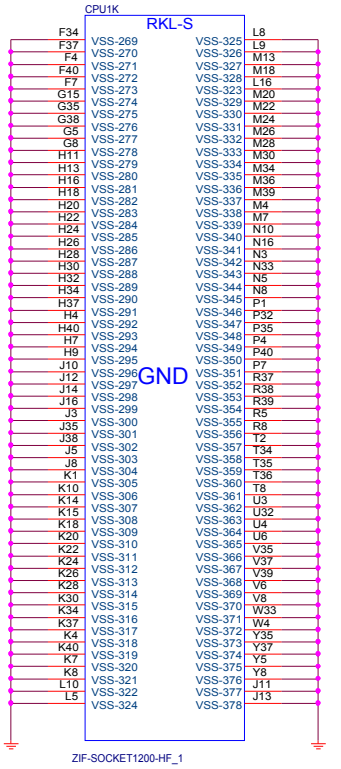

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Size: Custom	Document Description: CPU-GND	Rev: 10
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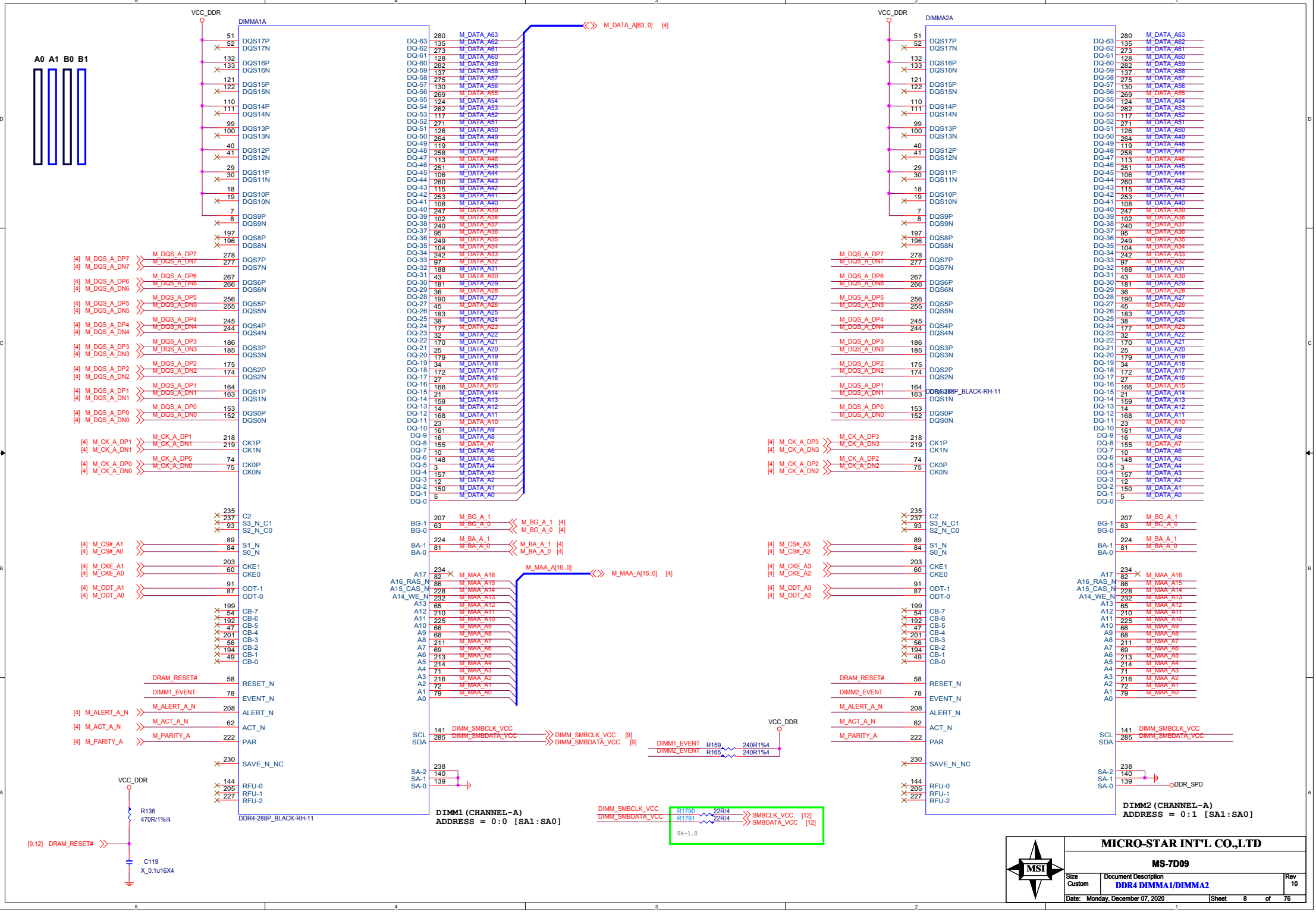
A0 A1 B0 B1
VCC_DDR
DIMMA1A
DDR4-288P_BLACK-RH-11
M_DATA_A[63..0] [4]
M_MAA_A[16..0] [4]
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
DIMMA2A
DDR4-288P_BLACK-RH-11
DIMM2(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
DIMM_SMBCLK_VCC [9]
DIMM_SMBDATA_VCC [9]
DIMM1_EVENT R159 240R1%4
DIMM2_EVENT R165 240R1%4
R1790 22R/4
R1791 22R/4
SMBCLK_VCC [12]
SMBDATA_VCC [12]
0A-1.0
DDR_SPD
R136
470R/1%/4
[9,12] DRAM_RESET#
C119
X_0.1u16X4
MICRO-STAR INT'L CO.,LTD
MS-7D09
Size Custom
Document Description
DDR4 DIMMA1/DIMMA2
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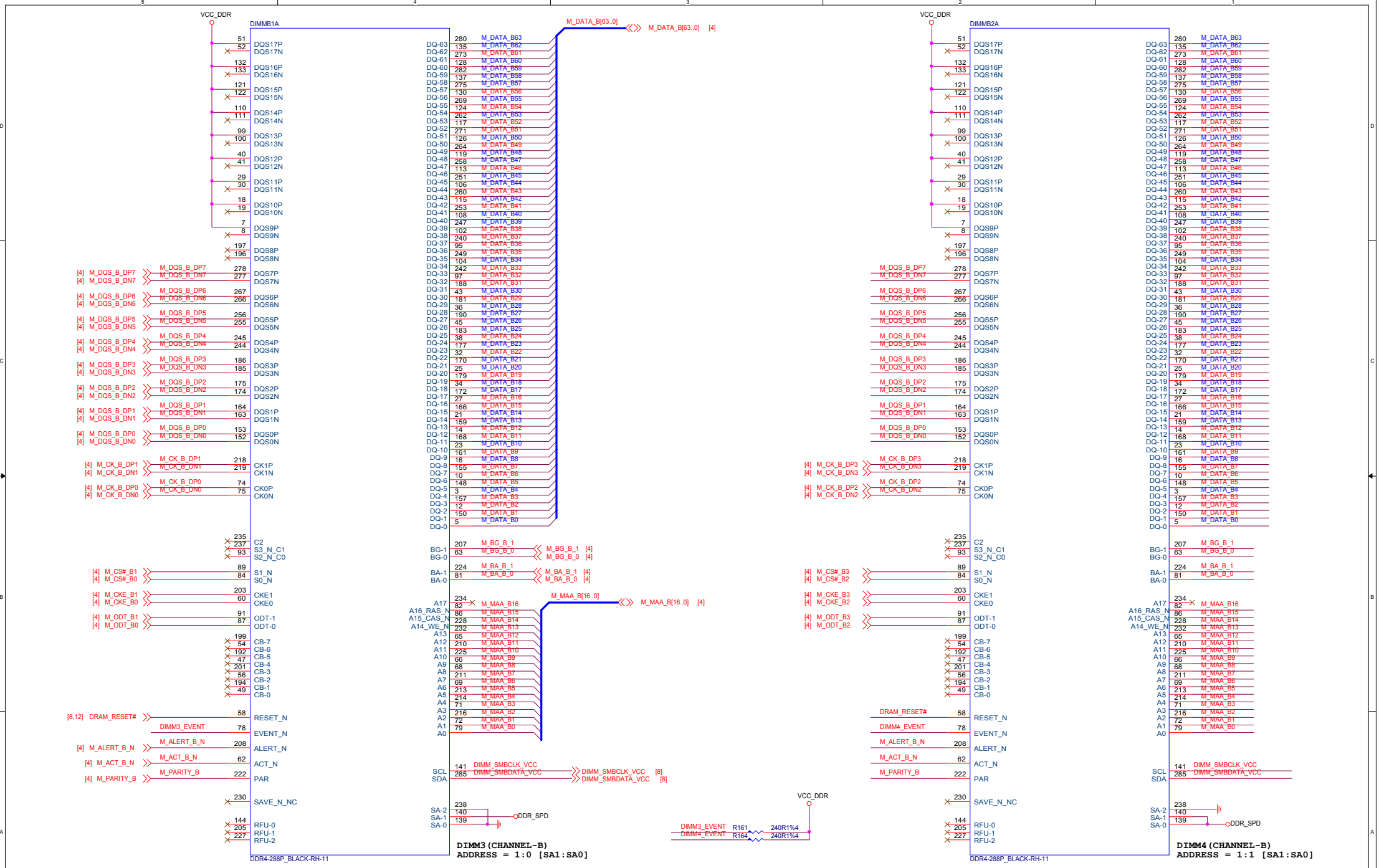

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D09	
Size: Custom	Document Description: DDR4 DIMMB1/DIMMB2	Rev: 10
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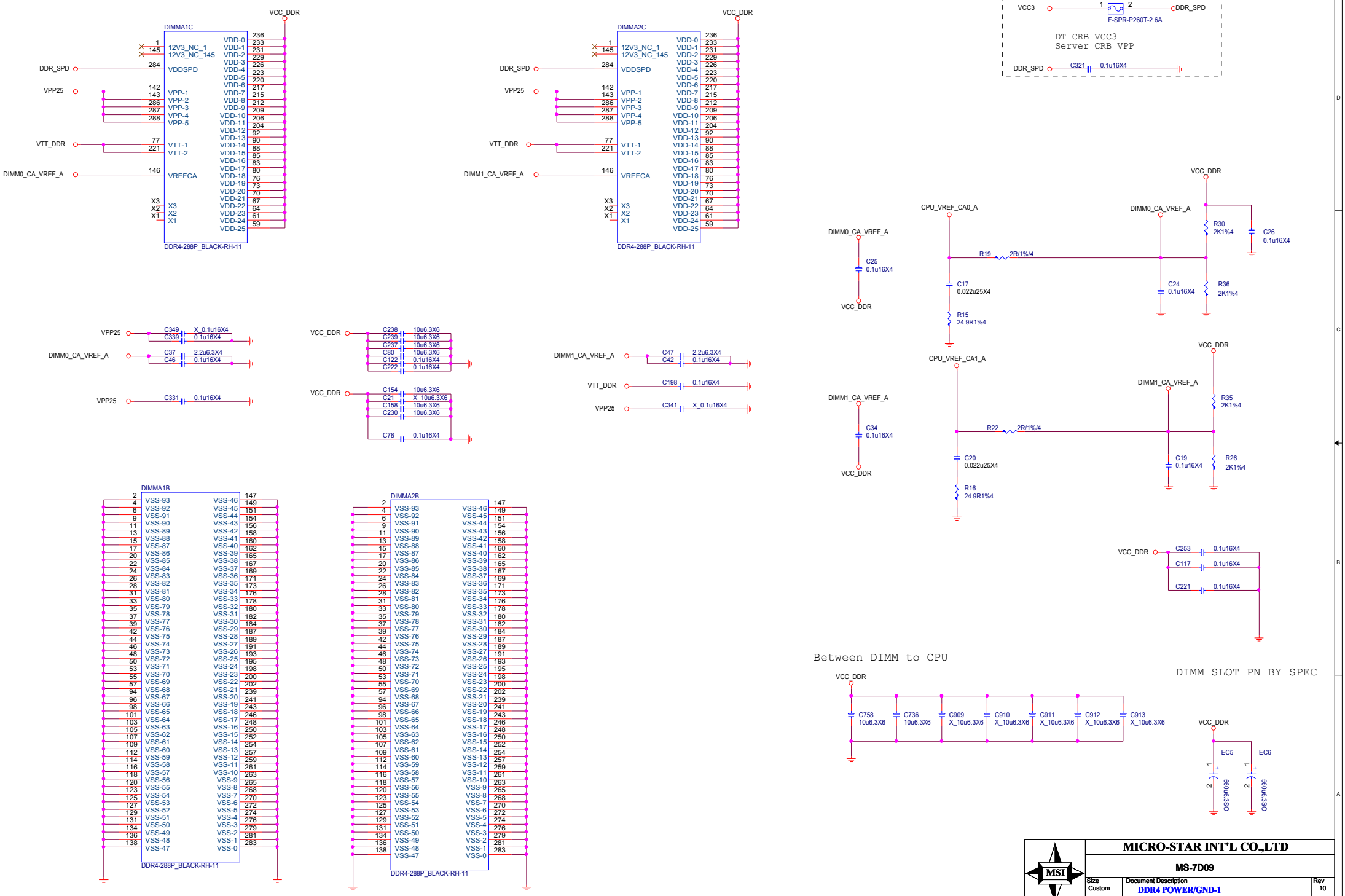
DIMMA1C
DDR4-288P_BLACK-RH-11
DIMMA2C
DDR4-288P_BLACK-RH-11
VCC_DDR
DDR_SPD
VPP25
VTT_DDR
DIMM0_CA_VREF_A
DIMM1_CA_VREF_A
VCC3
F4
F-SPR-P260T-2.6A
DT CRB VCC3
Server CRB VPP
C321 0.1u16X4
C349 X_0.1u16X4
C339 0.1u16X4
C37 2.2u6.3X4
C46 0.1u16X4
C331 0.1u16X4
C238 10u6.3X6
C239 10u6.3X6
C237 10u6.3X6
C80 10u6.3X6
C122 0.1u16X4
C222 0.1u16X4
C154 10u6.3X6
C21 X_10u6.3X6
C158 10u6.3X6
C230 10u6.3X6
C78 0.1u16X4
C47 2.2u6.3X4
C42 0.1u16X4
C198 0.1u16X4
C341 X_0.1u16X4
C25 0.1u16X4
CPU_VREF_CA0_A
R19 2R/1%/4
C17 0.022u25X4
R15 24.9R1%4
R30 2K1%4
C26 0.1u16X4
C24 0.1u16X4
R36 2K1%4
C34 0.1u16X4
CPU_VREF_CA1_A
R22 2R/1%/4
C20 0.022u25X4
R16 24.9R1%4
R35 2K1%4
C19 0.1u16X4
R26 2K1%4
C253 0.1u16X4
C117 0.1u16X4
C221 0.1u16X4
DIMMA1B
DDR4-288P_BLACK-RH-11
DIMMA2B
DDR4-288P_BLACK-RH-11
Between DIMM to CPU
C758 10u6.3X6
C736 10u6.3X6
C909 X_10u6.3X6
C910 X_10u6.3X6
C911 X_10u6.3X6
C912 X_10u6.3X6
C913 X_10u6.3X6
DIMM SLOT PN BY SPEC
EC5 560u6.3SO
EC6 560u6.3SO
MICRO-STAR INT'L CO.,LTD
MS-7D09
Size Custom
Document Description DDR4 POWER/GND-1
Rev 10
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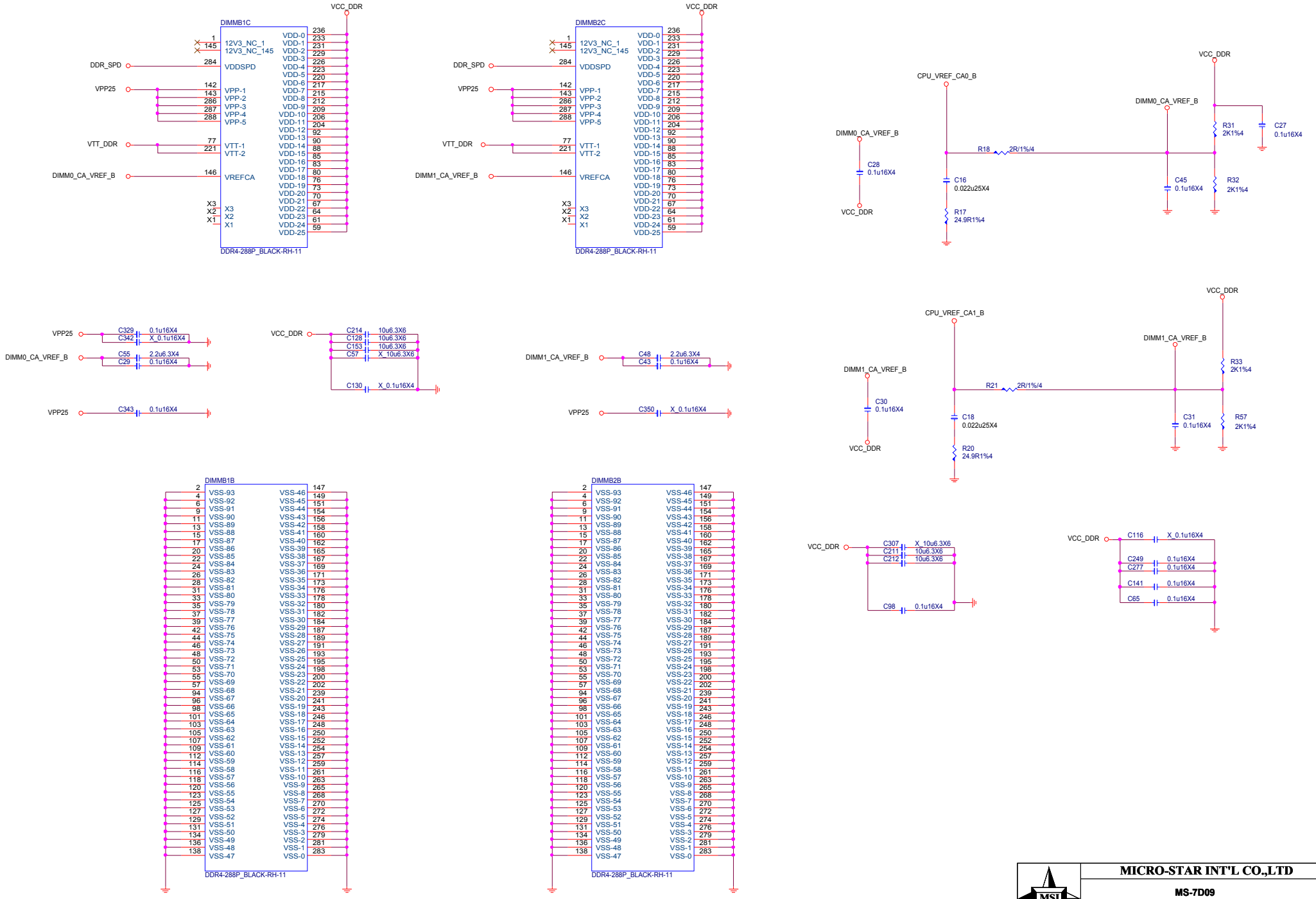

MICRO-STAR INT'L CO.,LTD	
MS-7D09	
Size: Custom	Document Description: DDR4 POWER/GND-2
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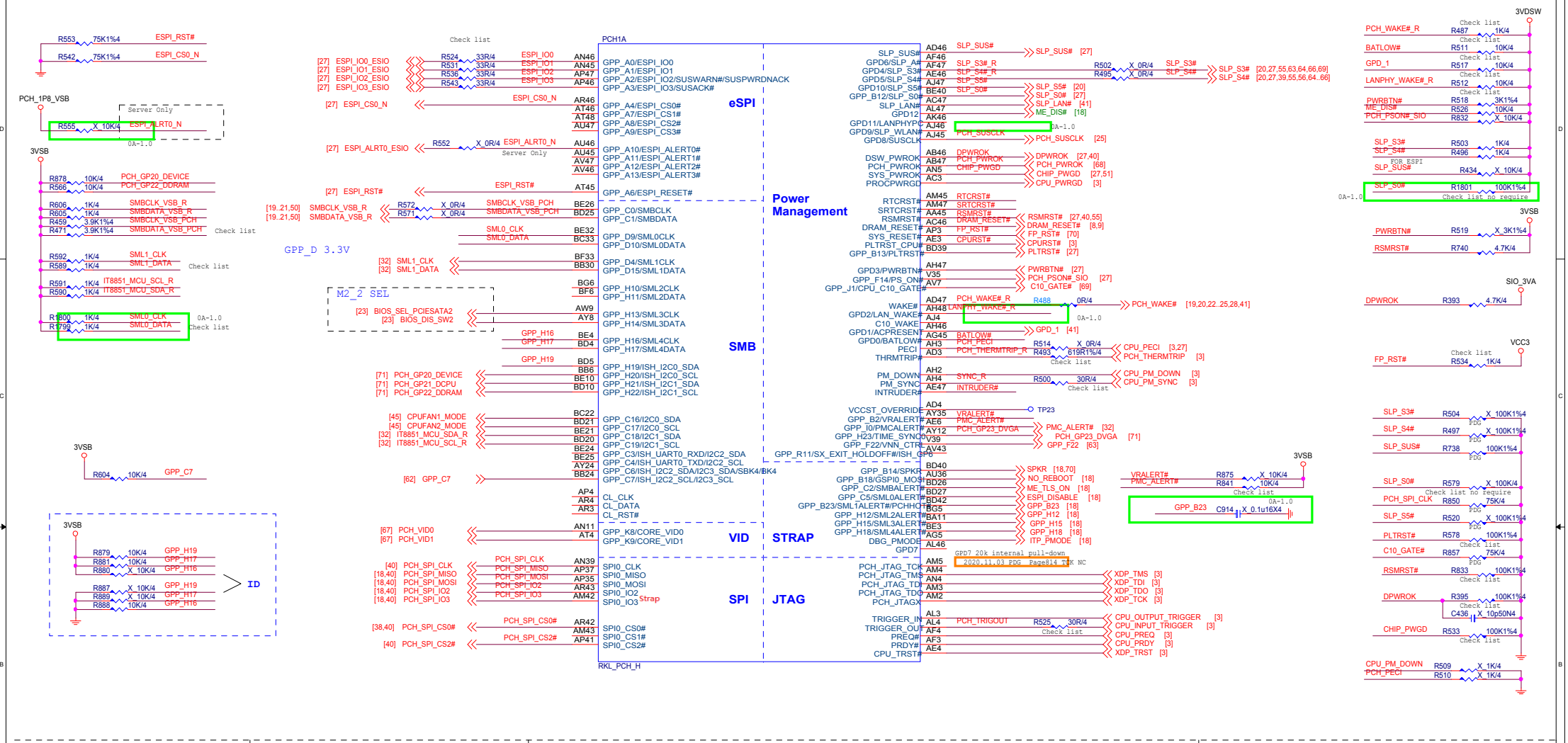
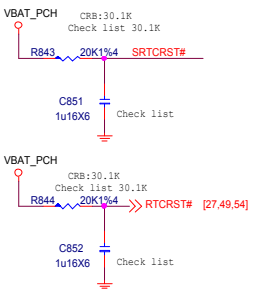
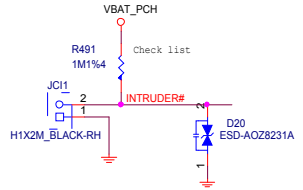
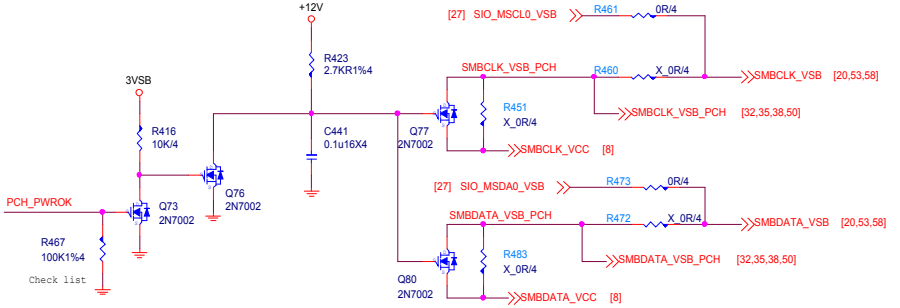


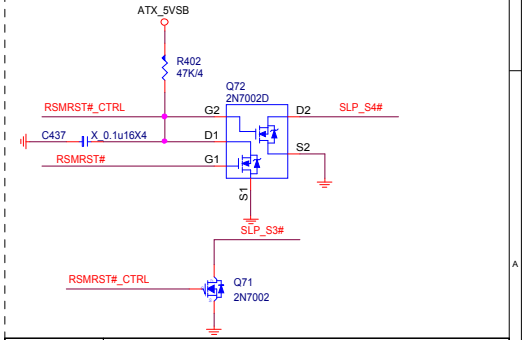
RTC



Chassis Intrusion







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Size: Custom	Document Description: PCH-LPC/SPI/SMBUS/MISC	Rev: 10
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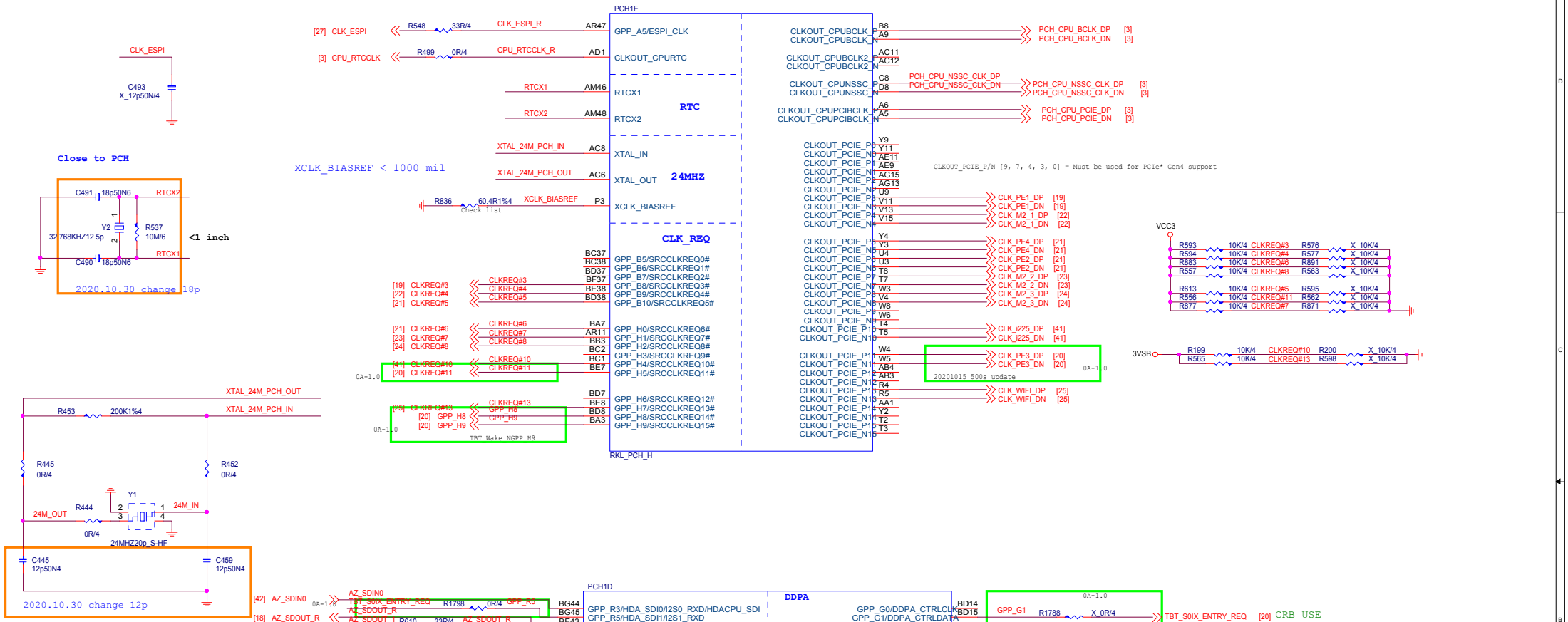
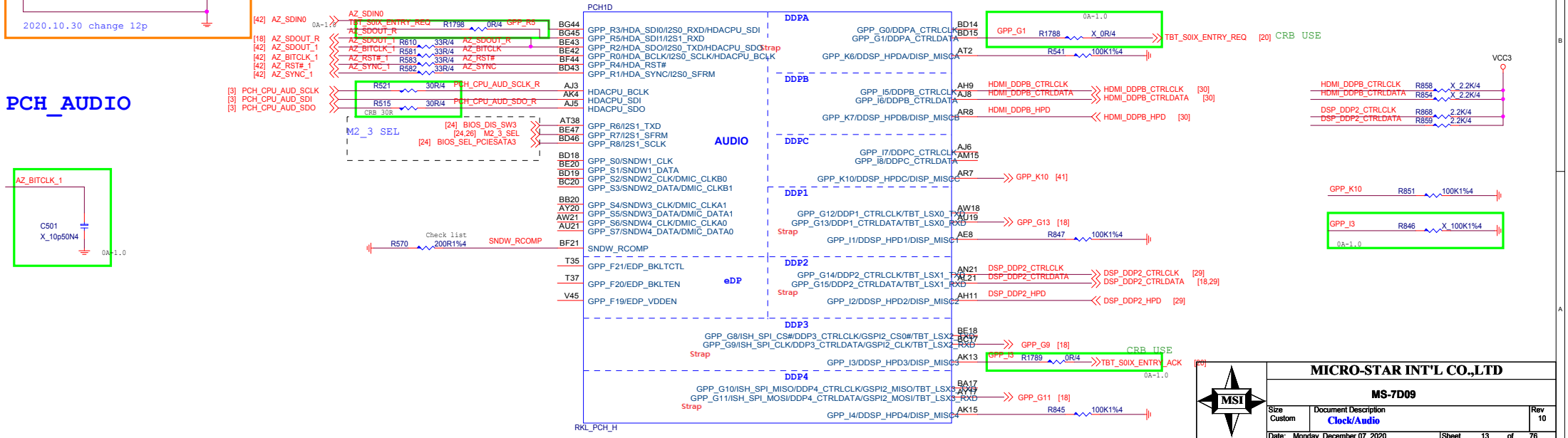
PCH_CLK



PCH_AUDIO



MICRO-STAR INT'L CO.,LTD	
MS-7D09	
Size: Custom	Document Description: Clock/Audio
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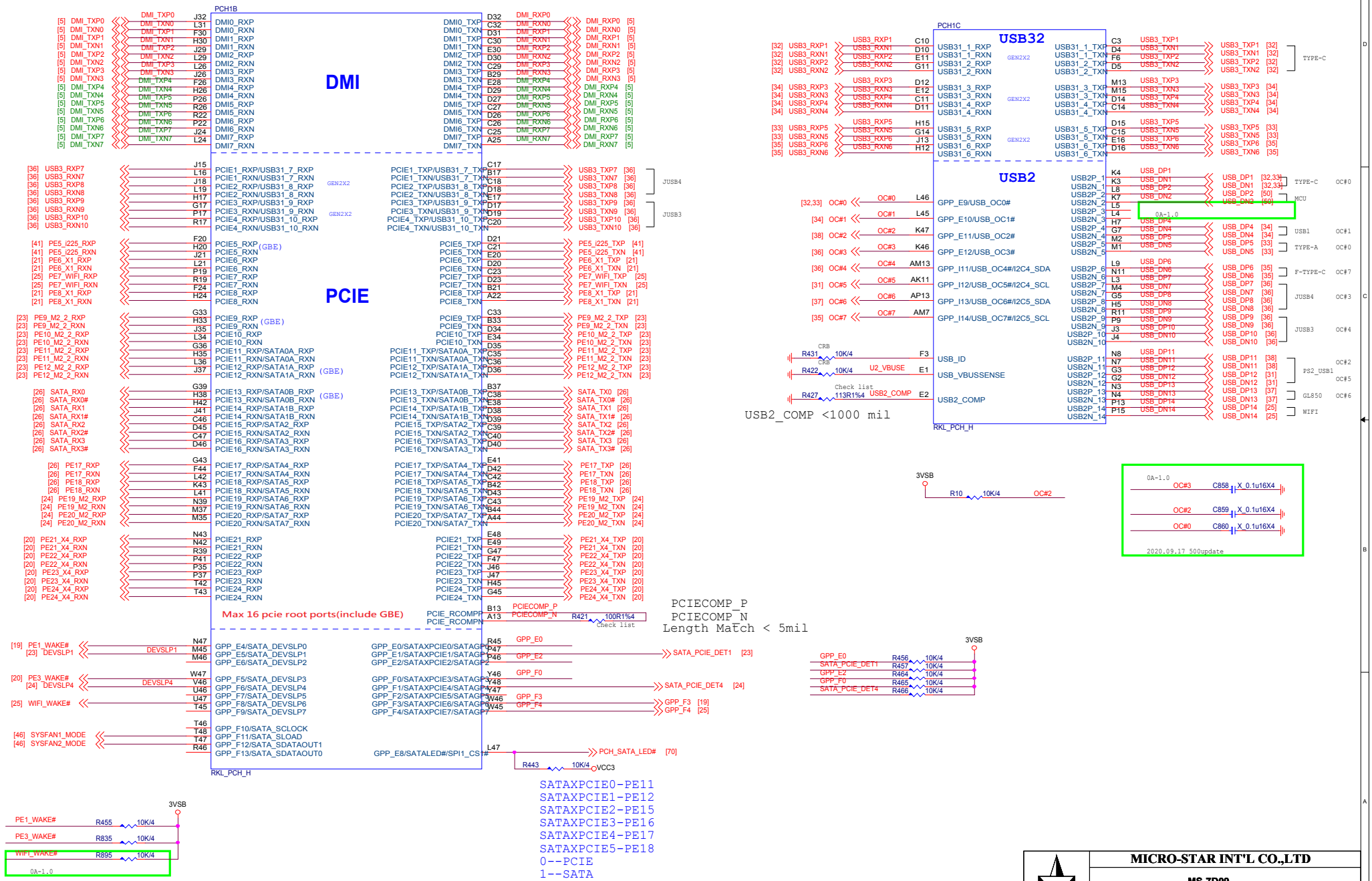

MICRO-STAR INT'L CO.,LTD		
MS-7D09		
Size: Custom	Document Description: PCH-DMI/PCIE/USB/SATA	Rev: 10
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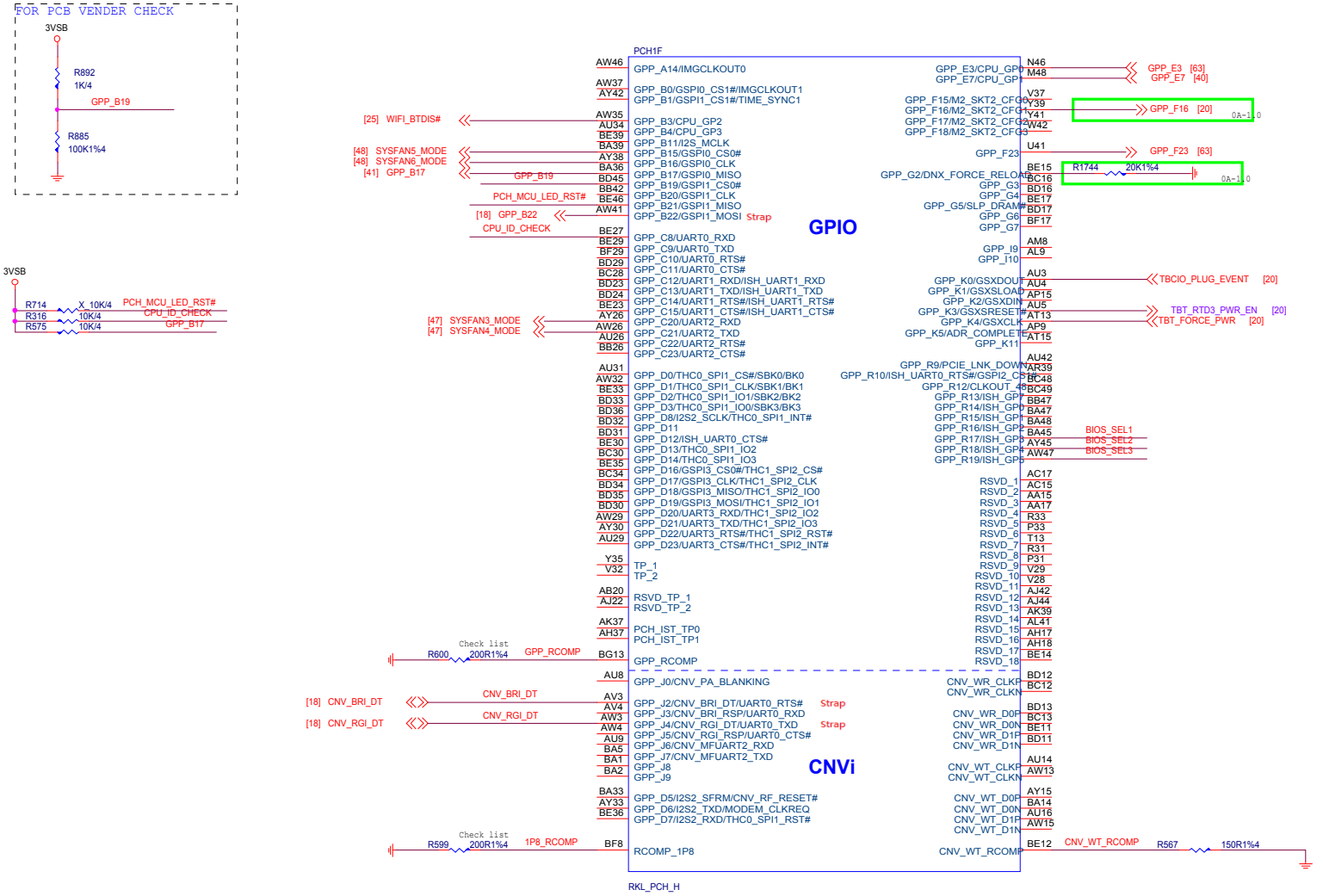
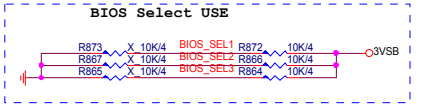
	BIOS_SEL1	BIOS_SEL2	BIOS_SEL3
WIFI	1	1	1
A PRO	0	1	1





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MS-7D09		
Size: Custom	Document Description: PCH-CNVI/GPIO	Rev: 10
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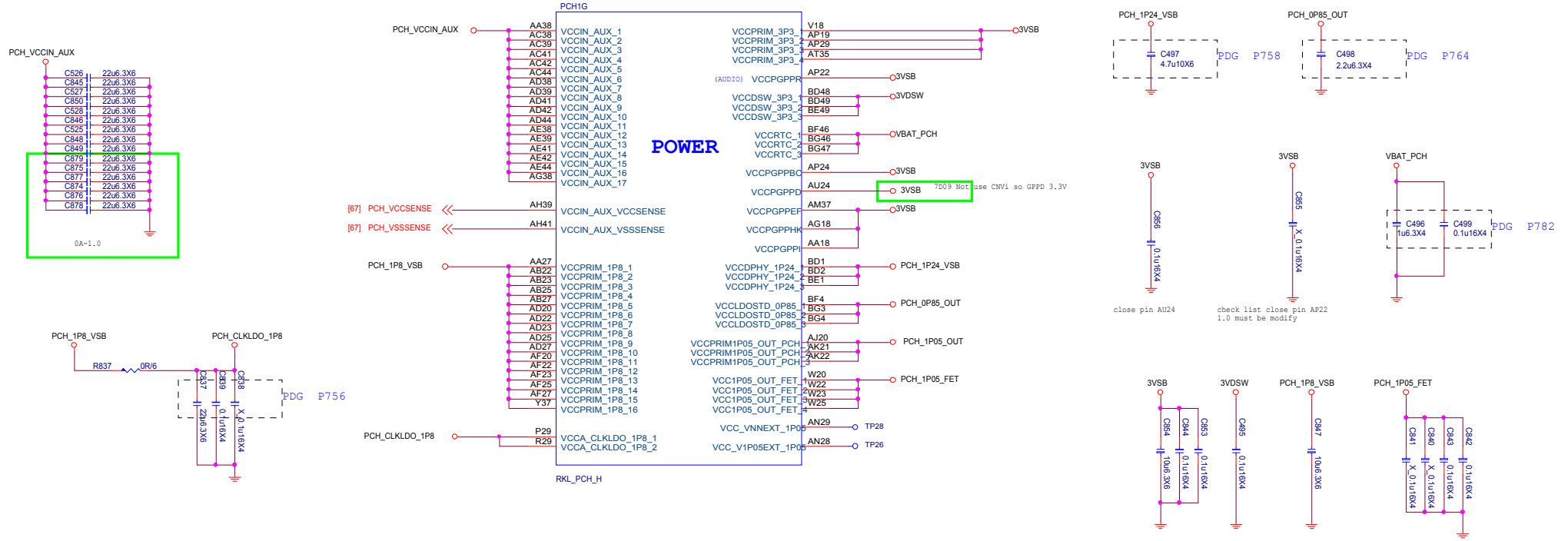

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PCH-Power	Rev: 10
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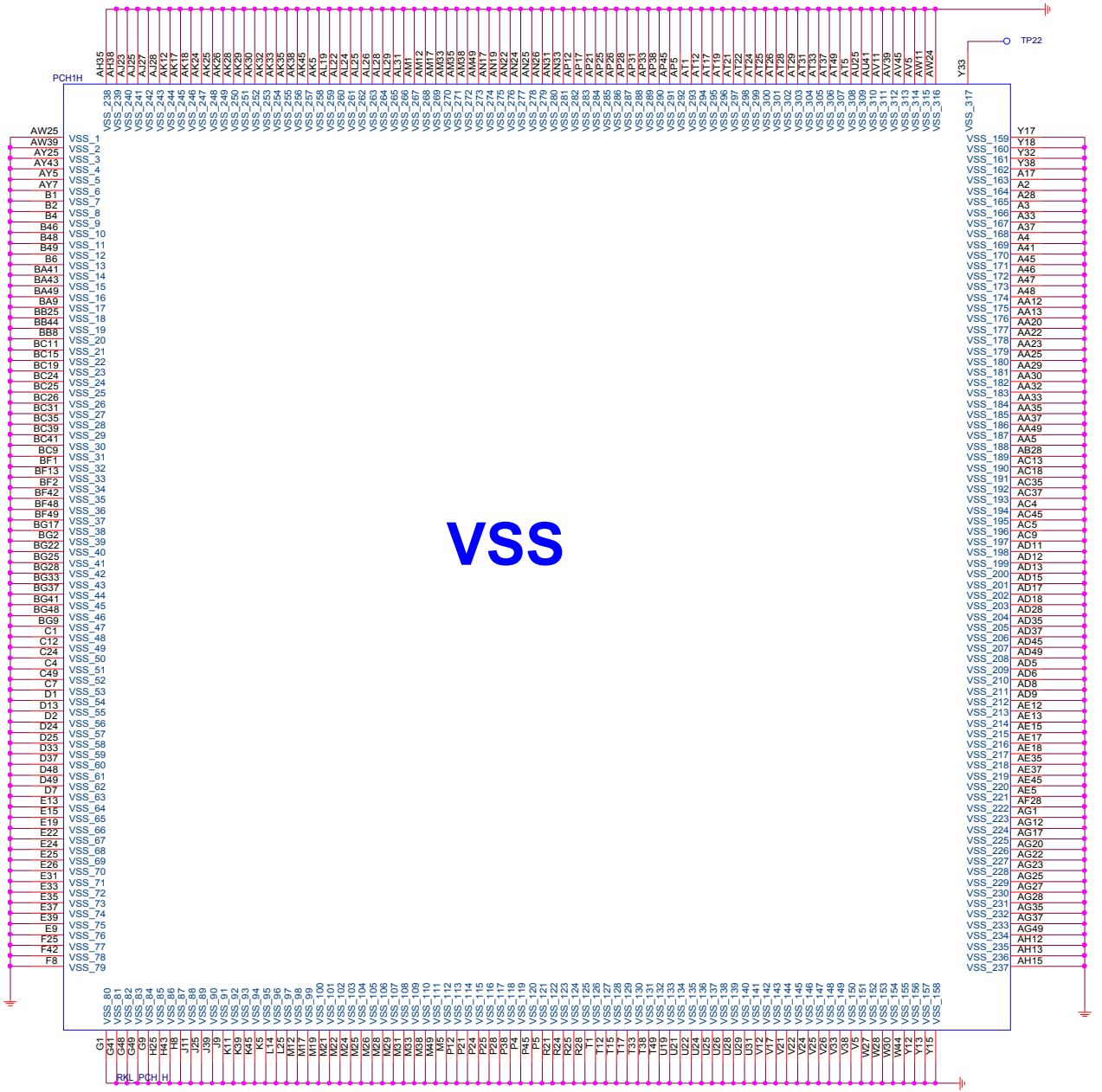

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: PCH-GND
Rev: 10	
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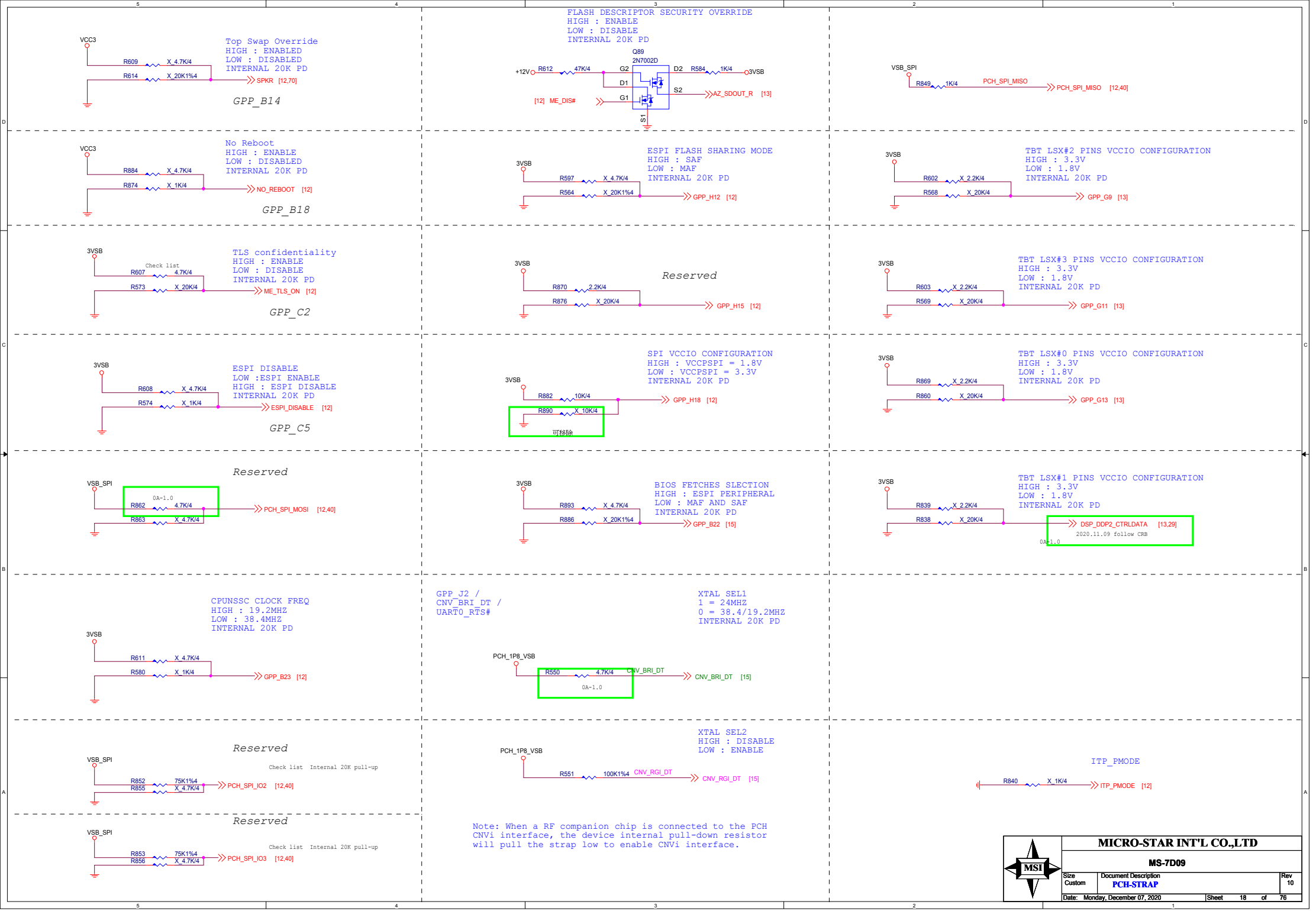
Top Swap Override
HIGH : ENABLED
LOW : DISABLED
INTERNAL 20K PD
VCC3
R609 X_4.7K/4
R614 X_20K1%4
SPKR [12,70]
GPP_B14
FLASH DESCRIPTOR SECURITY OVERRIDE
HIGH : ENABLE
LOW : DISABLE
INTERNAL 20K PD
Q89
2N7002D
+12V
R612 47K/4
G2
D1
G1
S1
D2
S2
R584 1K/4
3VSB
AZ_SDOUT_R [13]
[12] ME_DIS#
VSB_SPI
R849 1K/4
PCH_SPI_MISO
PCH_SPI_MISO [12,40]
No Reboot
HIGH : ENABLE
LOW : DISABLED
INTERNAL 20K PD
R884 X_4.7K/4
R874 X_1K/4
NO_REBOOT [12]
GPP_B18
ESPI FLASH SHARING MODE
HIGH : SAF
LOW : MAF
INTERNAL 20K PD
R597 X_4.7K/4
R564 X_20K1%4
GPP_H12 [12]
TBT LSX#2 PINS VCCIO CONFIGURATION
HIGH : 3.3V
LOW : 1.8V
INTERNAL 20K PD
R602 X_2.2K/4
R568 X_20K/4
GPP_G9 [13]
TLS confidentiality
HIGH : ENABLE
LOW : DISABLE
INTERNAL 20K PD
Check list
R607 4.7K/4
R573 X_20K/4
ME_TLS_ON [12]
GPP_C2
Reserved
R870 2.2K/4
R876 X_20K/4
GPP_H15 [12]
TBT LSX#3 PINS VCCIO CONFIGURATION
HIGH : 3.3V
LOW : 1.8V
INTERNAL 20K PD
R603 X_2.2K/4
R569 X_20K/4
GPP_G11 [13]
ESPI DISABLE
LOW :ESPI ENABLE
HIGH : ESPI DISABLE
INTERNAL 20K PD
R608 X_4.7K/4
R574 X_1K/4
ESPI_DISABLE [12]
GPP_C5
SPI VCCIO CONFIGURATION
HIGH : VCCPSPI = 1.8V
LOW : VCCPSPI = 3.3V
INTERNAL 20K PD
R882 10K/4
R890 X_10K/4
可移除
GPP_H18 [12]
TBT LSX#0 PINS VCCIO CONFIGURATION
HIGH : 3.3V
LOW : 1.8V
INTERNAL 20K PD
R869 X_2.2K/4
R860 X_20K/4
GPP_G13 [13]
Reserved
0A-1.0
R862 4.7K/4
R863 X_4.7K/4
PCH_SPI_MOSI [12,40]
BIOS FETCHES SLECTION
HIGH : ESPI PERIPHERAL
LOW : MAF AND SAF
INTERNAL 20K PD
R893 X_4.7K/4
R886 X_20K1%4
GPP_B22 [15]
TBT LSX#1 PINS VCCIO CONFIGURATION
HIGH : 3.3V
LOW : 1.8V
INTERNAL 20K PD
R839 X_2.2K/4
R838 X_20K/4
DSP_DDP2_CTRLDATA [13,29]
2020.11.09 follow CRB
0A-1.0
CPUNSSC CLOCK FREQ
HIGH : 19.2MHZ
LOW : 38.4MHZ
INTERNAL 20K PD
R611 X_4.7K/4
R580 X_1K/4
GPP_B23 [12]
GPP_J2 /
CNV_BRI_DT /
UART0_RTS#
XTAL SEL1
1 = 24MHZ
0 = 38.4/19.2MHZ
INTERNAL 20K PD
PCH_1P8_VSB
R550 4.7K/4
CNV_BRI_DT
0A-1.0
CNV_BRI_DT [15]
Reserved
Check list Internal 20K pull-up
R852 75K1%4
R855 X_4.7K/4
PCH_SPI_IO2 [12,40]
XTAL SEL2
HIGH : DISABLE
LOW : ENABLE
R551 100K1%4
CNV_RGI_DT
CNV_RGI_DT [15]
ITP_PMODE
R840 X_1K/4
ITP_PMODE [12]
Reserved
R853 75K1%4
R856 X_4.7K/4
PCH_SPI_IO3 [12,40]
Note: When a RF companion chip is connected to the PCH
CNVi interface, the device internal pull-down resistor
will pull the strap low to enable CNVi interface.
MICRO-STAR INT'L CO.,LTD
MS-7D09
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Document Description
PCH-STRAP
Rev 10
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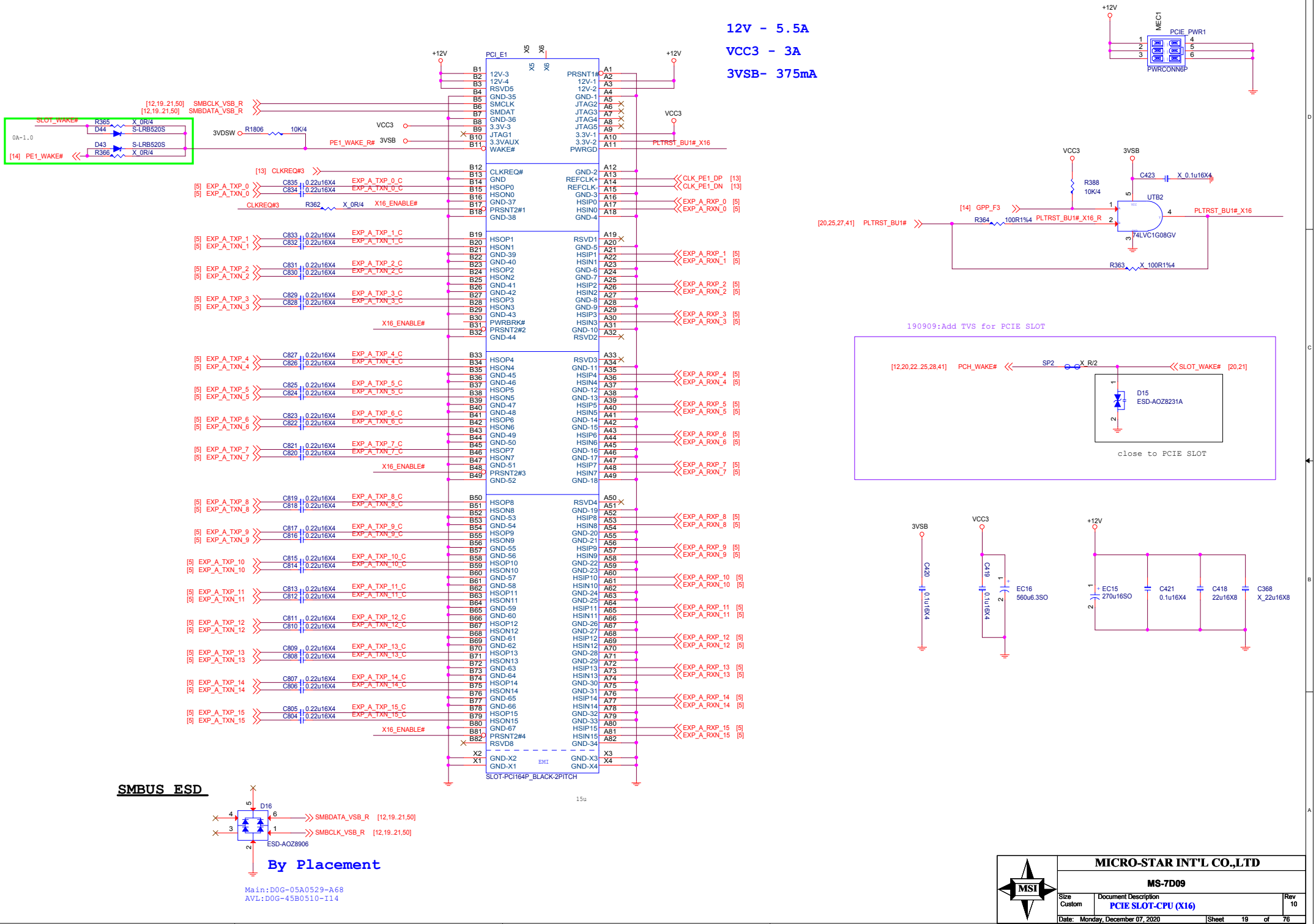
12V - 5.5A
VCC3 - 3A
3VSB- 375mA
PCI_E1
SLOT-PCI164P_BLACK-2PITCH
SMBUS ESD
D16
ESD-AOZ8906
By Placement
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14
MEC1
PCIE_PWR1
PWRCONN6P
UTB2
74LVC1G08GV
190909:Add TVS for PCIE SLOT
D15
ESD-AOZ8231A
close to PCIE SLOT
MICRO-STAR INT'L CO.,LTD
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PCIE SLOT-CPU (X16)
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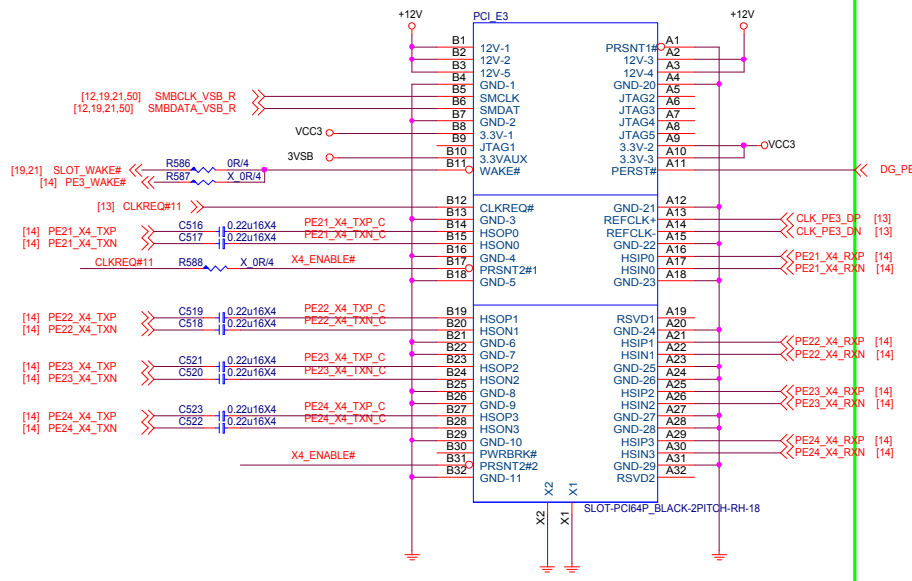
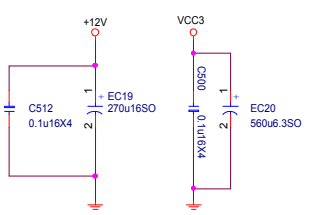
PCI_Express X4 Slot

12V - 2.1A

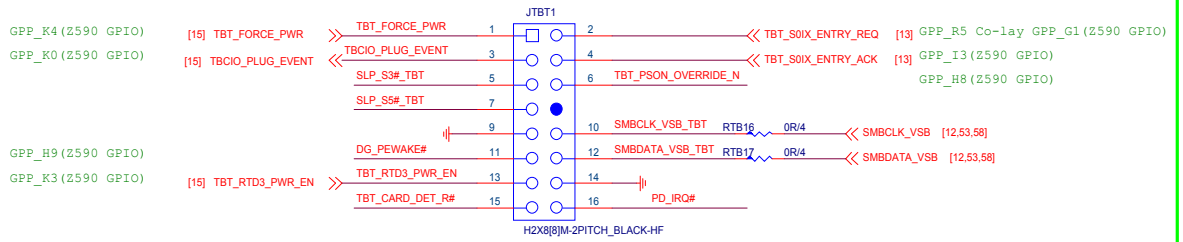
VCC3 - 3A

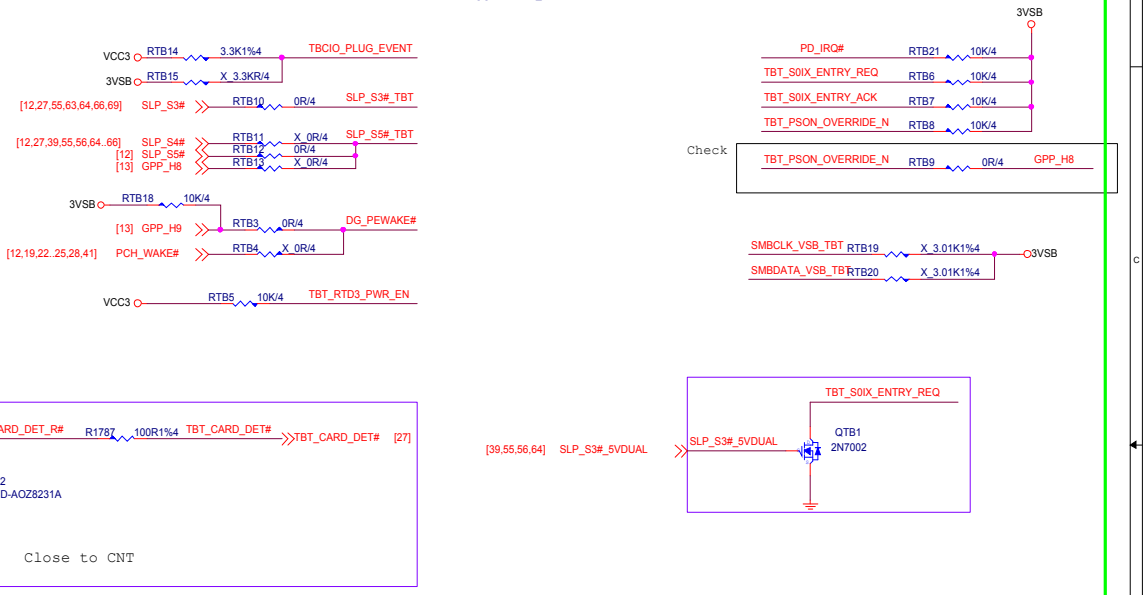
3VSBV - 375mA





JTBT





0A-1.0

MICRO-STAR INT'L CO.,LTD			
MS-7D09			
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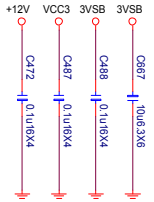
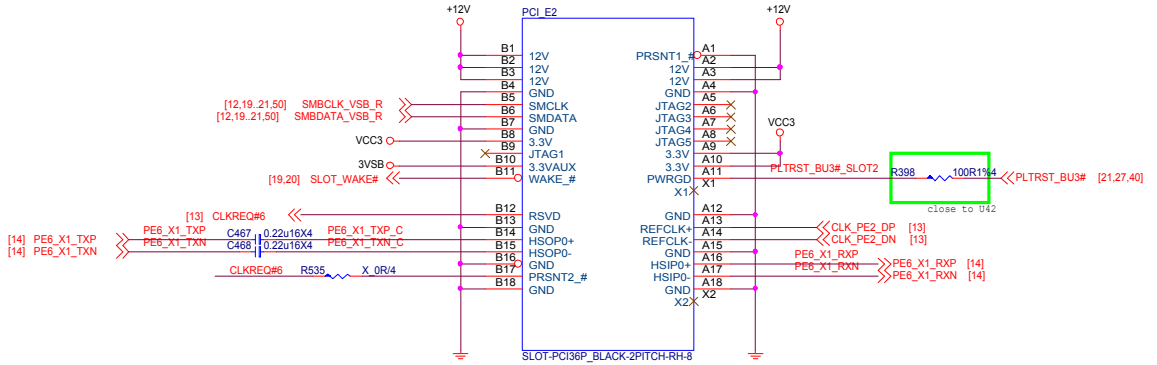
PCH PCIE X1 Slot

12V - 0.5A

VCC3 - 3A

3VSBV - 20mA



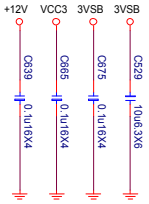


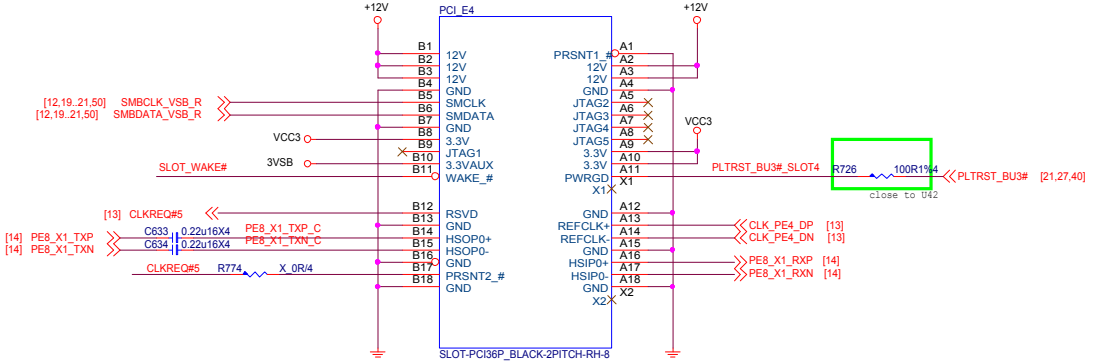
PCH PCIE X1 Slot

12V - 0.5A

VCC3 - 3A

3VSBV - 20mA





MICRO-STAR INT'L CO.,LTD		
MS-7D09		
Size: Custom	Document Description: PCIE SLOT-PCH (X1)	Rev: 10
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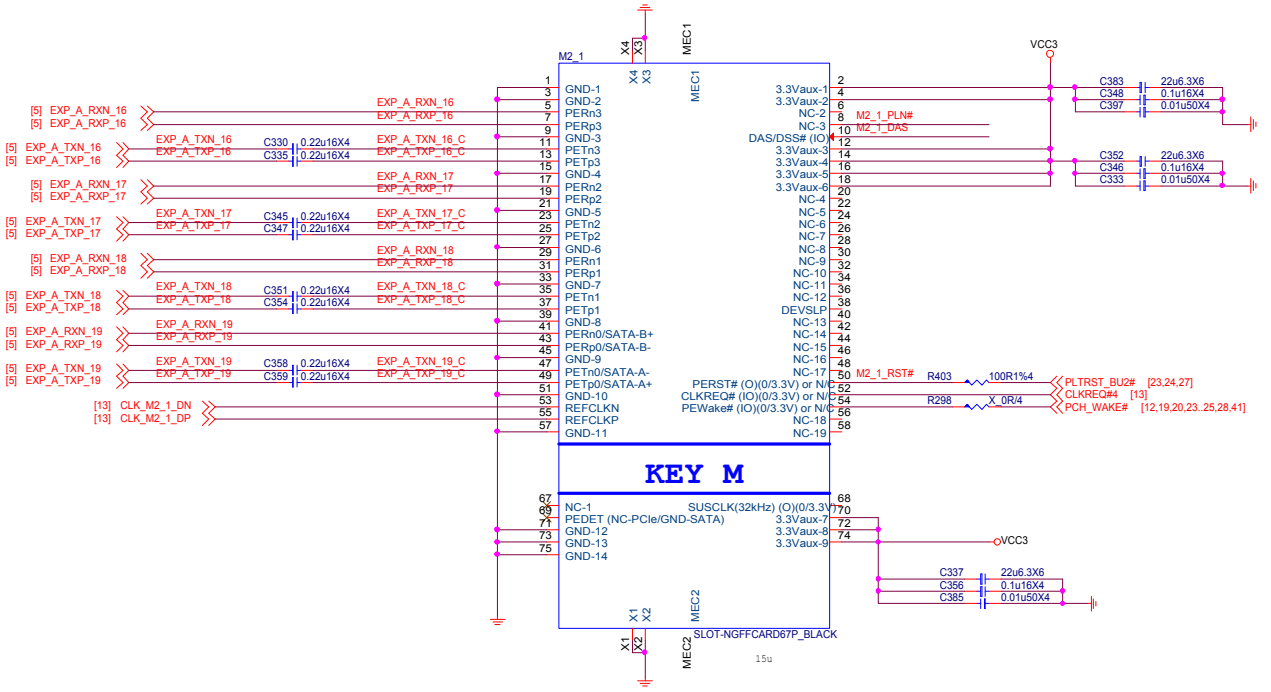
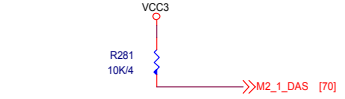
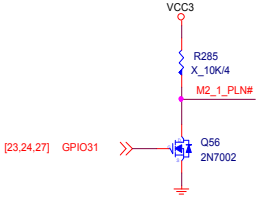
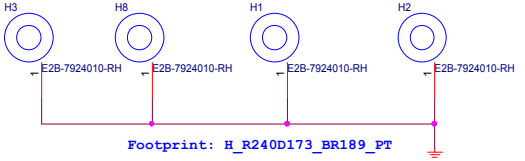
M2_1-from CPU









MICRO-STAR INT'L CO.,LTD		
MS-7D09		
Size: Custom	Document Description: M.2_1-SLOT1	Rev: 10
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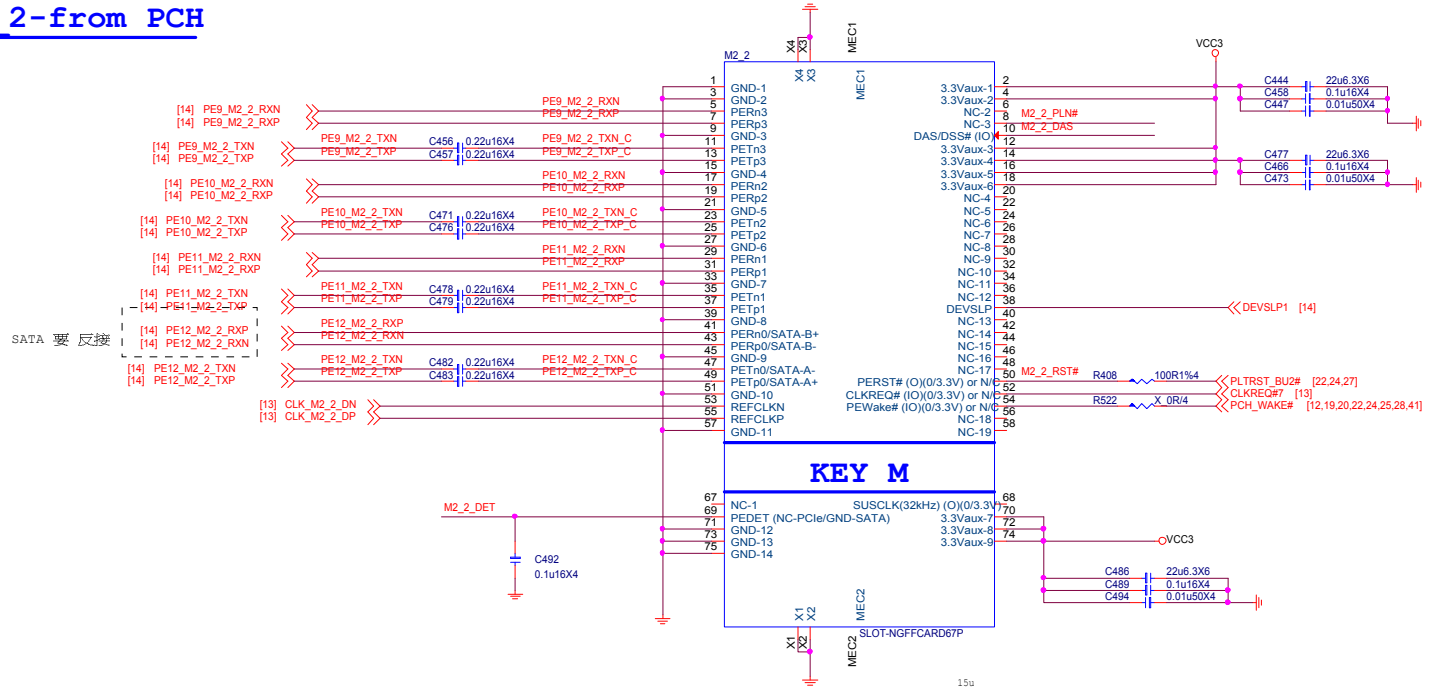
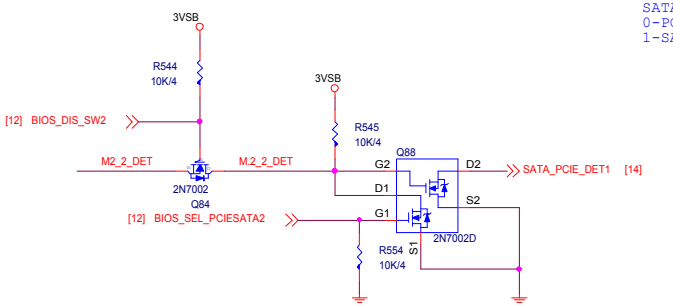
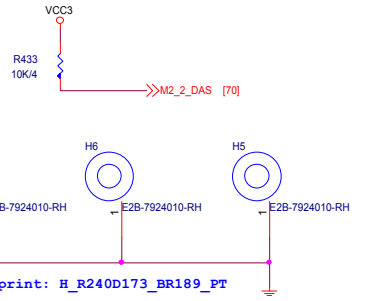
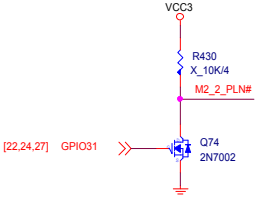
M2_2-from PCH



SATA_PCIE_DET1
0-PCIE
1-SATA







BIOS_MODE

BIOS_DIS_SW2 GPP_H14	BIOS_SEL_PCIESATA2 GPP__H13	Mode
GPO(0)	GPO(1)	M2-SATA
GPO(0)	GPO(0)	M2-PCIE
GPI	GPI	AUTO

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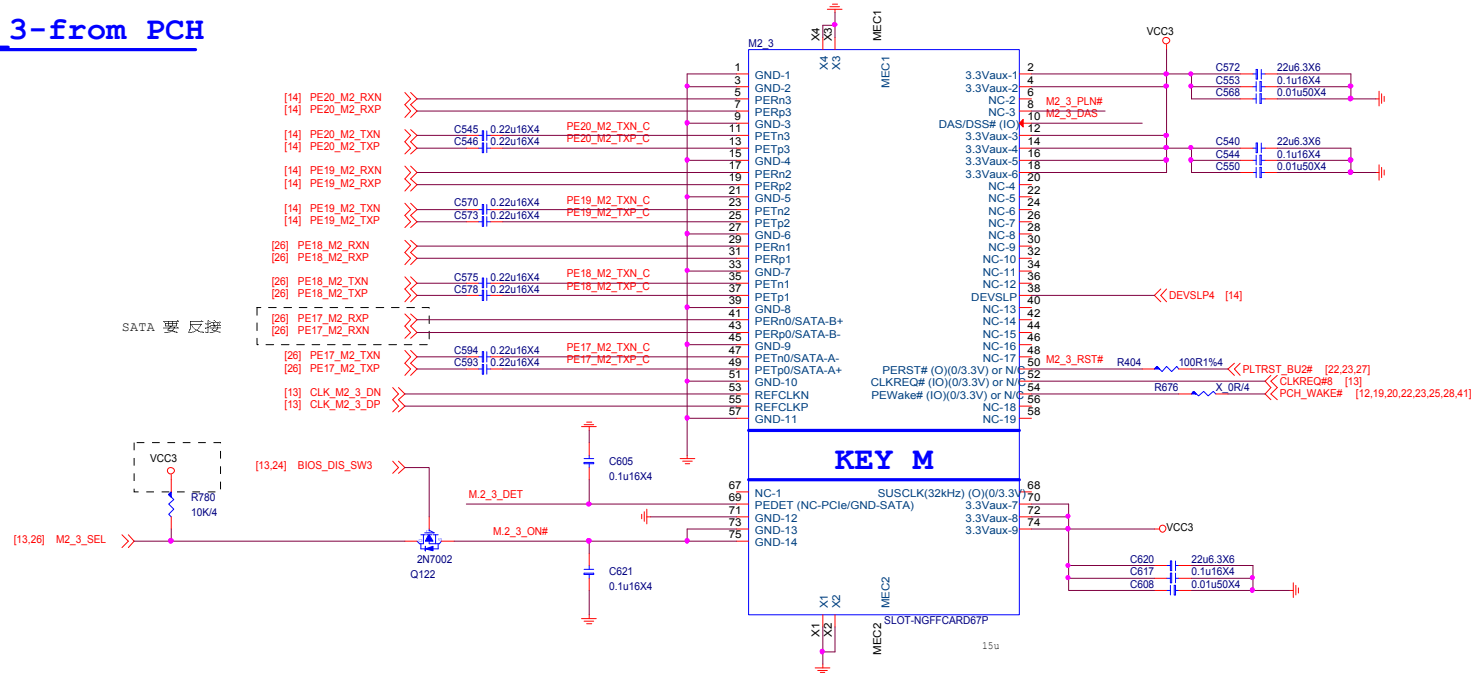
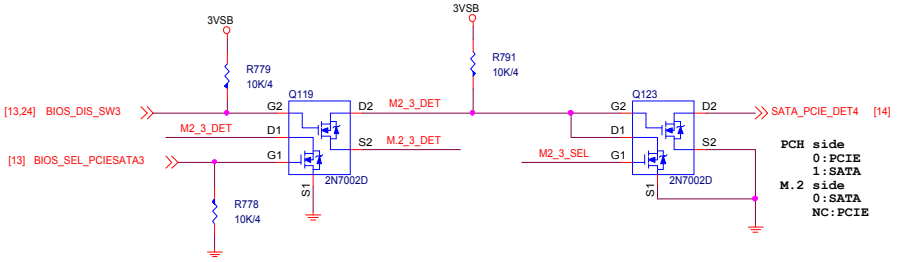
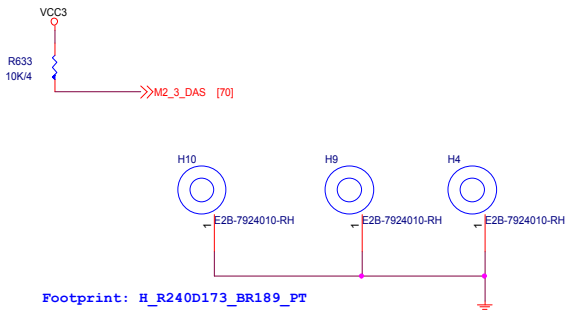
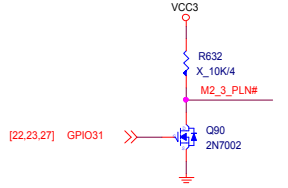
M2_3-from PCH



SATA_PCIE_DET4
0-PCIE
1-SATA







BIOS_MODE

GPP_R6 GPP_R7 GPP_R8

BIOS_DIS_SW	M2_3_SEL	BIOS_SEL_PCIESATA3	Mode
GPI(1)	GPI(1)	GPI(0)	AUTO
0	1	0	SATA5
0	0	1	M2-SATA
0	0	0	M2-PCIE

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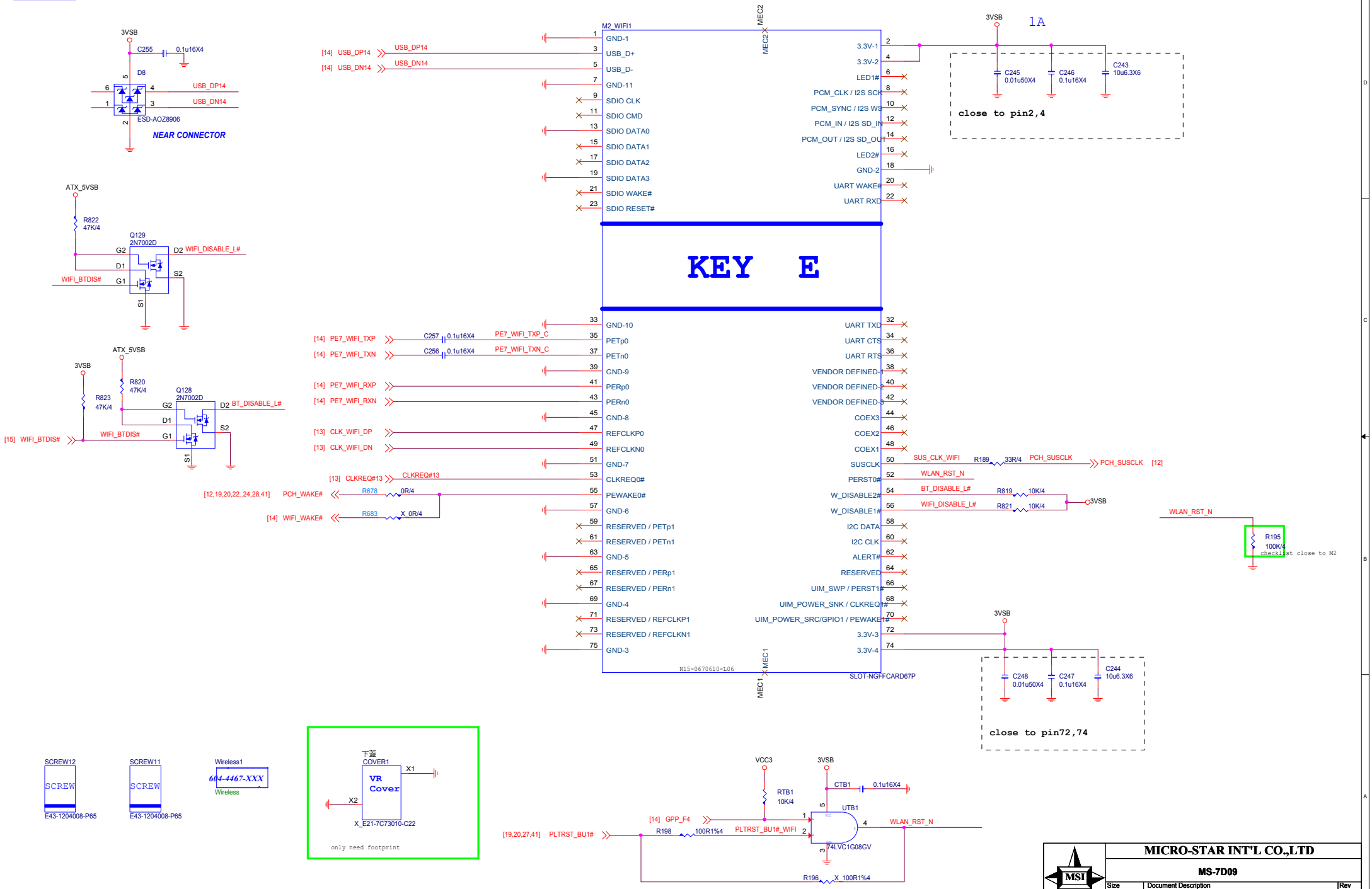
WIFI



MICRO-STAR INT'L CO.,LTD		
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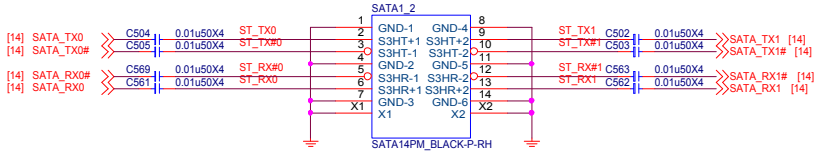
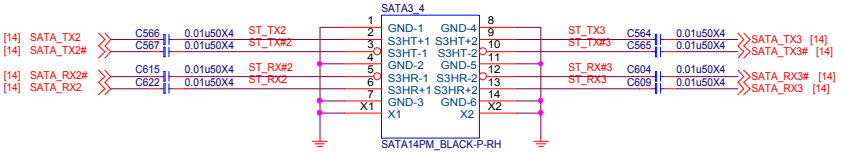
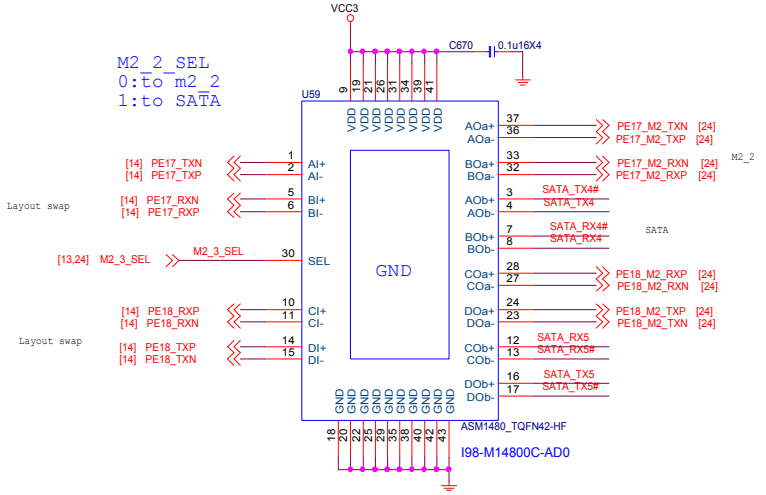
SATA 6G PORT 0.1



SATA 6G PORT 2.3





MICRO-STAR INT'L CO.,LTD		
MS-7D09		
Size: Custom	Document Description: SATA Connector	Rev: 10
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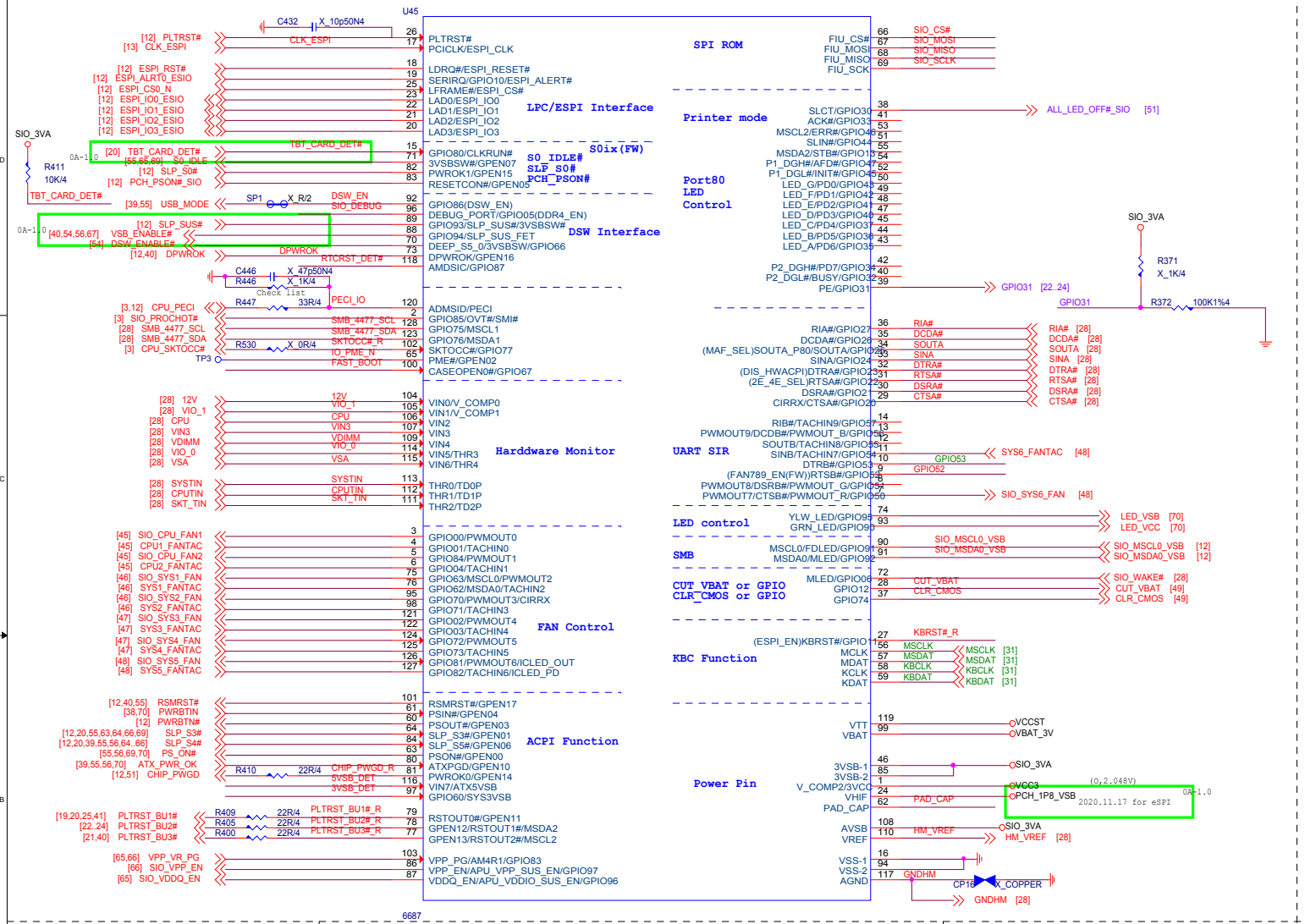
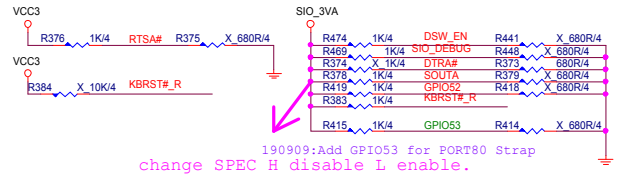
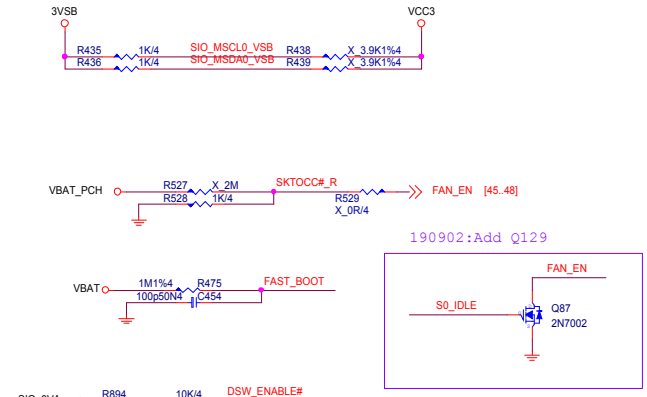
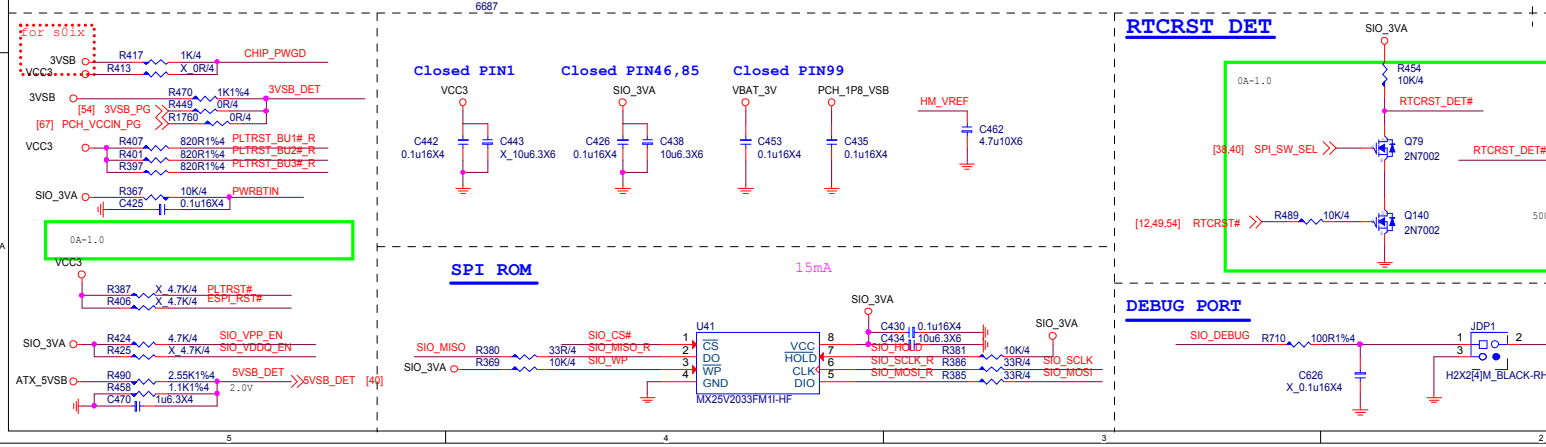


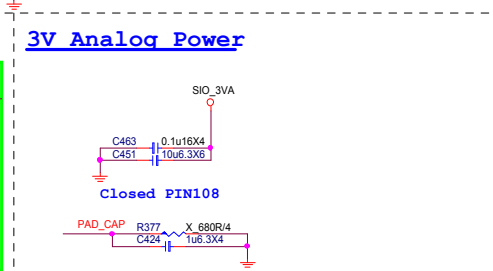
POWER ON STRAPPING PIN FOR NCT6687

PIN	NAME	Circuit NAME	0	1	Strap Point
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR4_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789 disable	FAN789 enable	3VA
PIN	NAME	Circuit NAME	VCC3	3VA	Strap Point
27	ESPI_EN	KBRST#	LPC	ESPI	VCC3 or 3VA
10	P80_EN	GPIO53	Default PORT80	Default GPI	3VA









MICRO-STAR INT'L CO.,LTD

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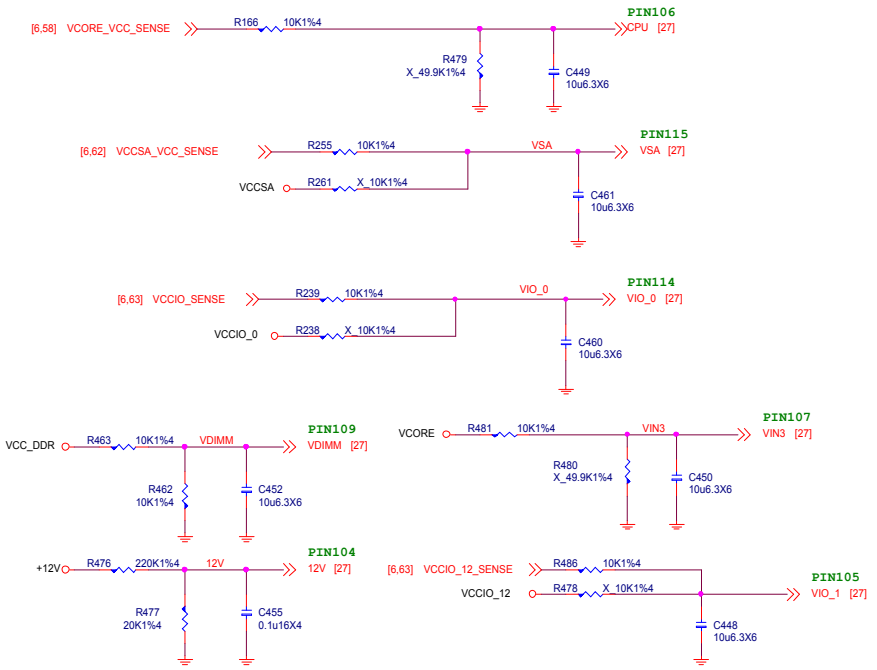
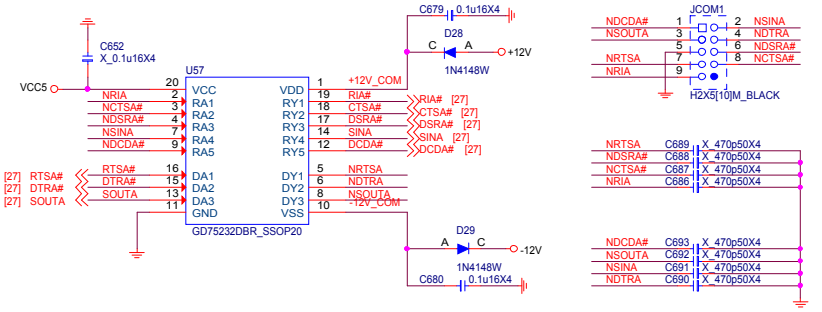
HW Monitor - Voltage

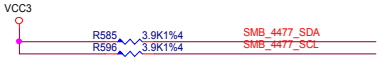
SIO HM Voltage Over 2V will Not Detect



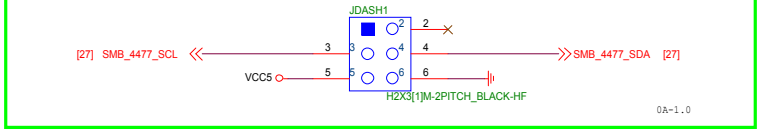
Serial Port 1



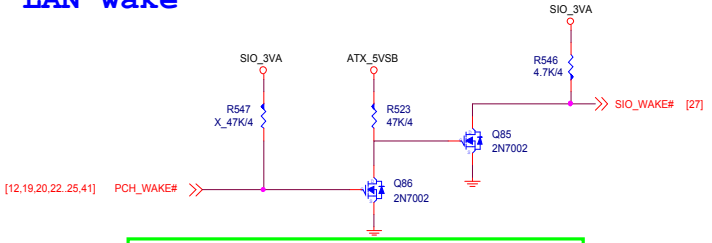
JDASH1



For 4472 Card

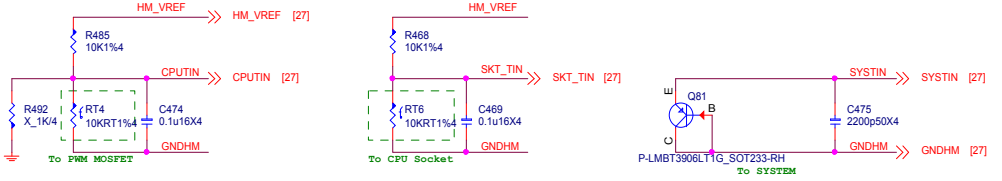


for LAN wake



0A-1.0 Remove LANPHY_WAKE# control

Thermal



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D09	
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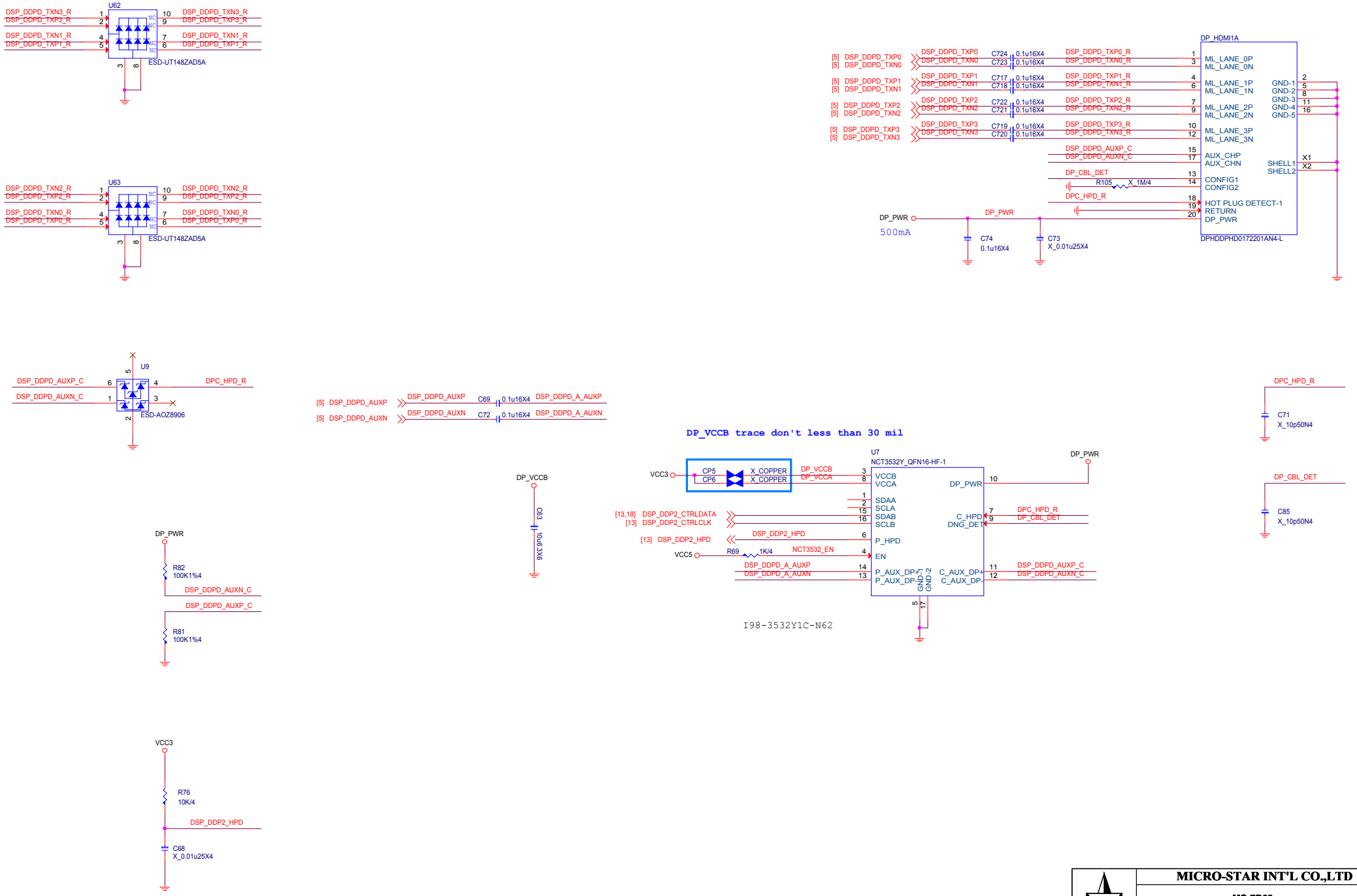

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: DP	Rev: 10
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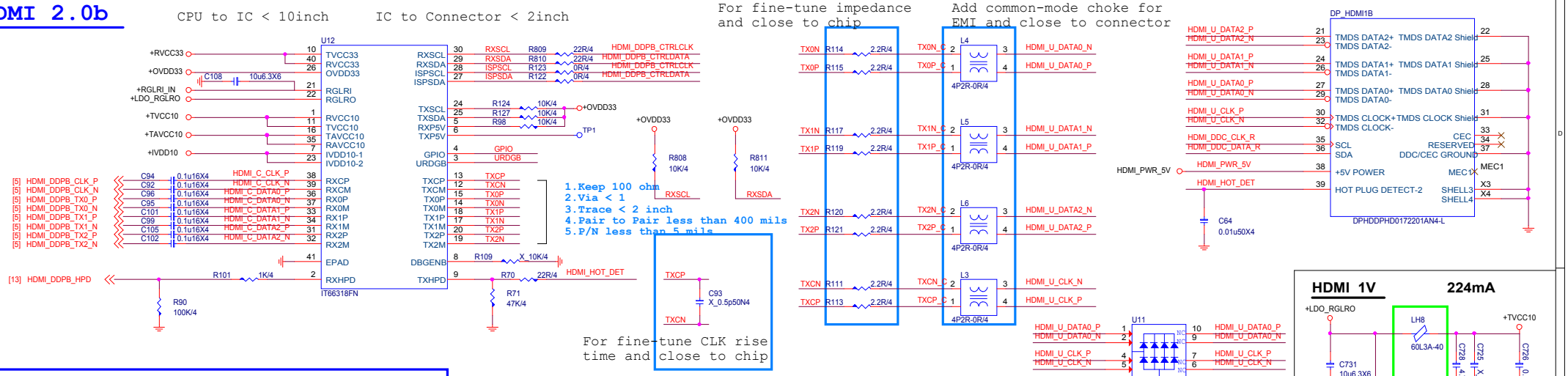
HDMI 2.0b

CPU to IC < 10inch IC to Connector < 2inch

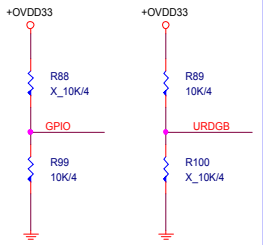
For fine-tune impedance and close to chip

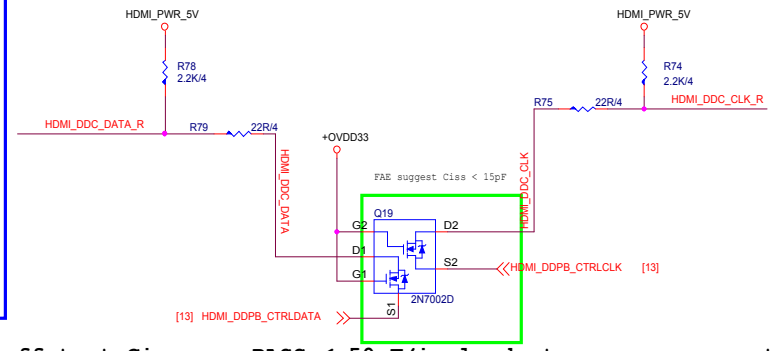
Add common-mode choke for EMI and close to connector



Reserved Trapping Setting

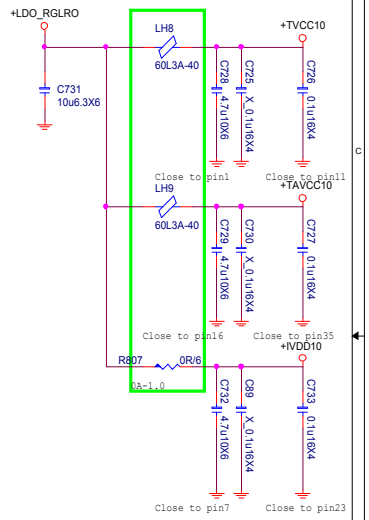
Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1



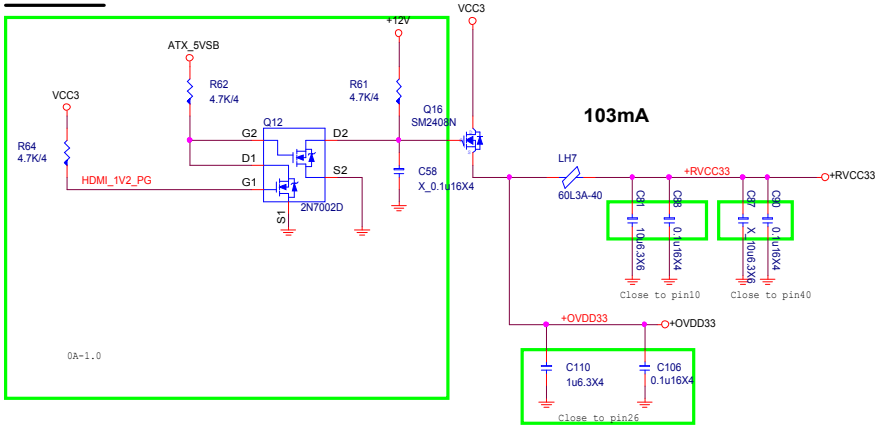


Power off test Ciss can PASS < 50pF(incloude trace,mos,connector).
but,Power ON test Ciss,You should choose Mos less then Ciss < 15pF.
SA test Ciss condition is Power off now.

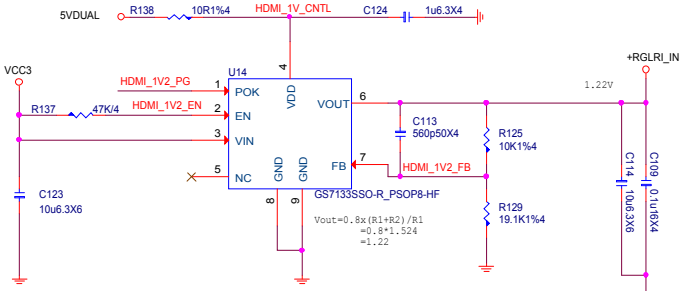
HDMI 1V 224mA



HDMI 3.3V

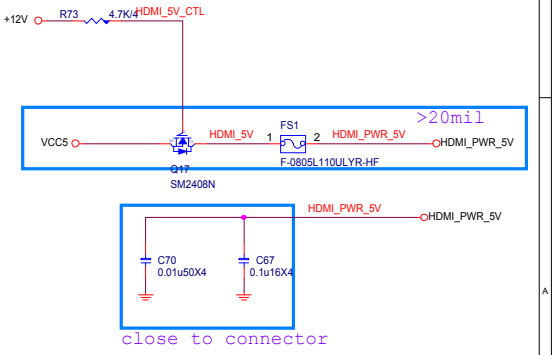


HDMI 1.2V



Power Loss=(Vin-Vou)*Iout
=(3.3-1.2)*0.224
=2.1*0.224
=0.48W < 1.33W

HDMI 5V



MICRO-STAR INT'L CO.,LTD		
MS-7D09		
Size: Custom	Document Description: HDMI-1	Rev: 10
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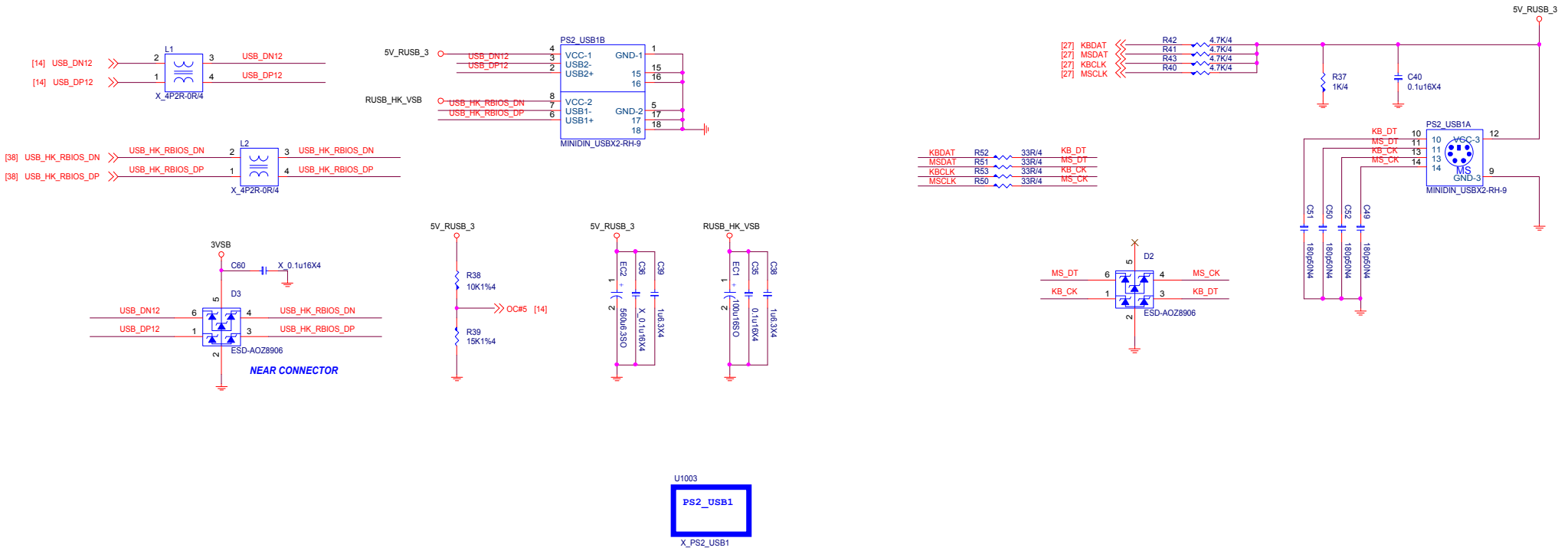
Rear PS2_USB2.0 0.5A+0.5A

PS2



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MS-7D09		
Size: Custom	Document Description: Rear PS2_USB1	Rev: 10
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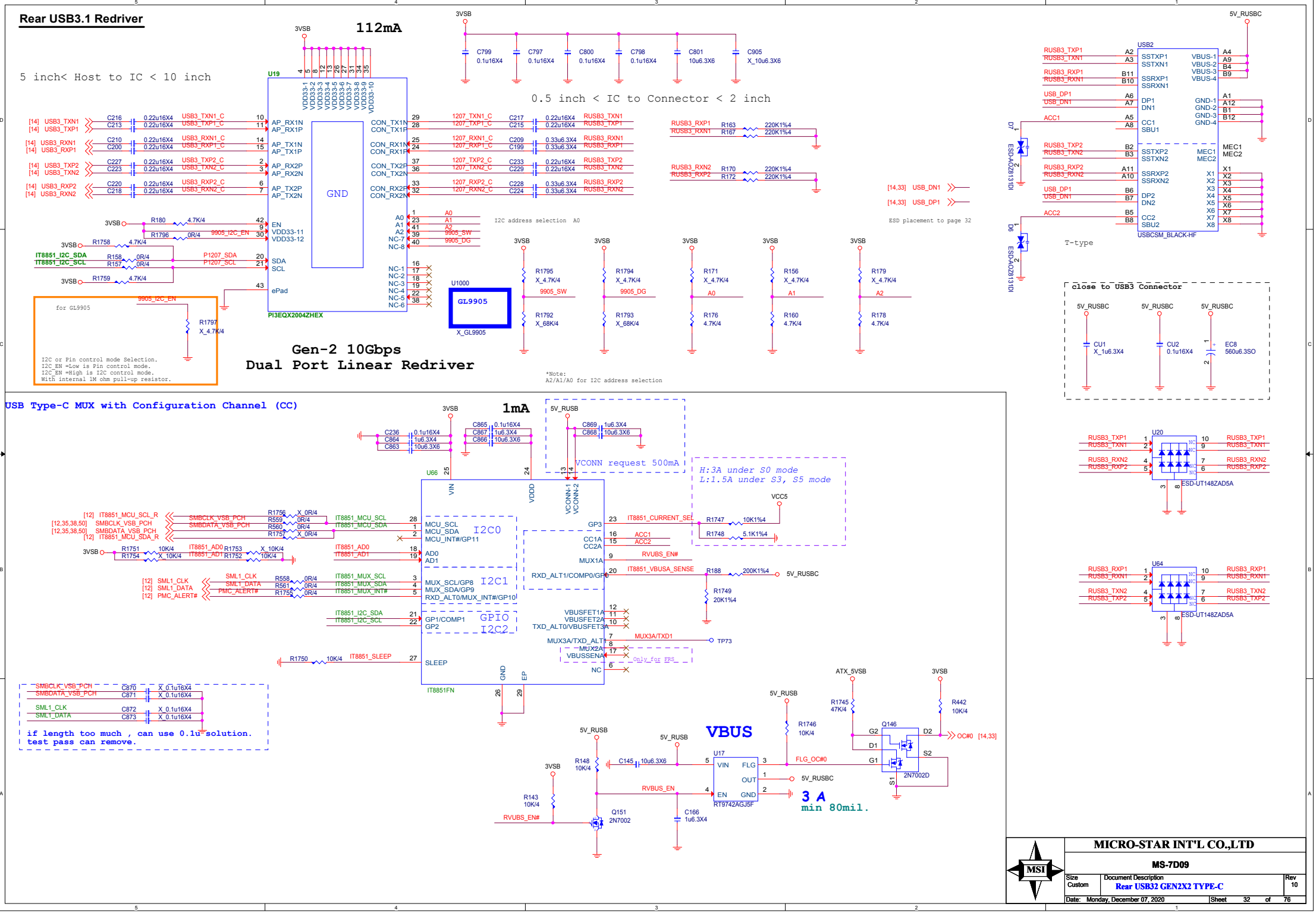
Rear USB3.1 Redriver



MICRO-STAR INT'L CO.,LTD

MS-7D09

Size	Document Description	Rev
Custom	Rear USB32 GEN2X2 TYPE-C	10

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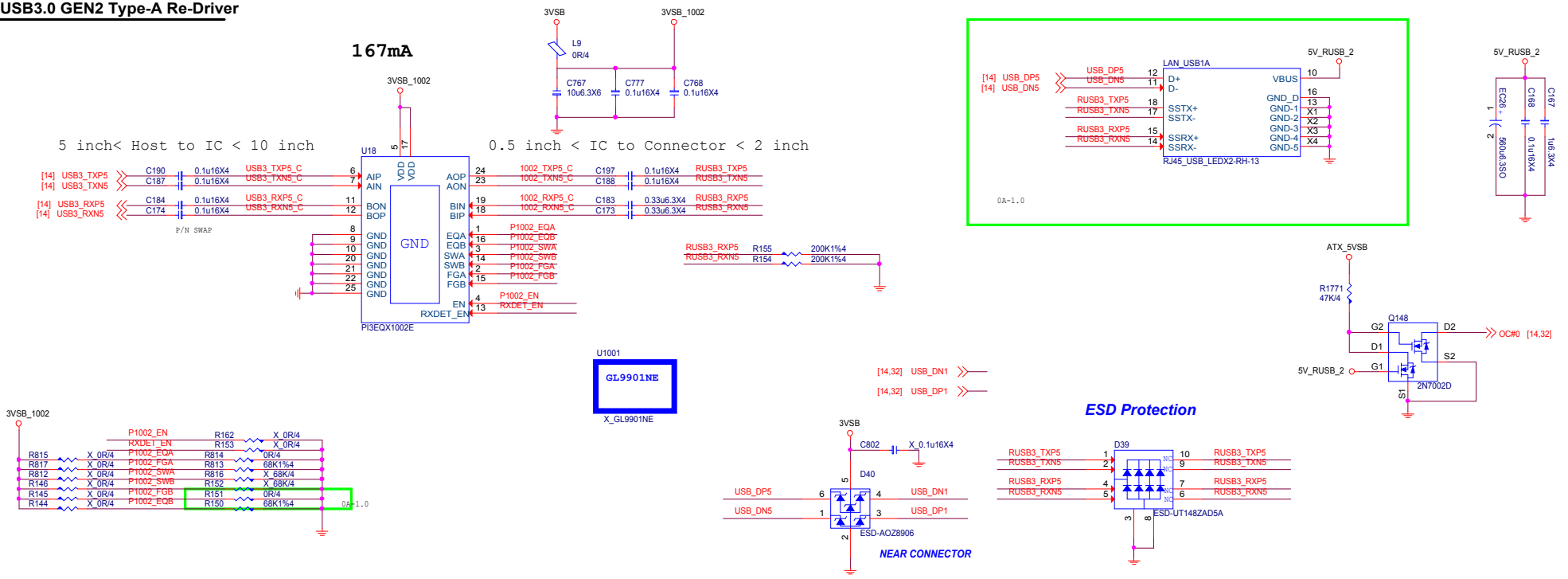
REAR USB3.0 GEN2 Type-A Re-Driver



Receiver Detection Setting

RXDET_EN	Setting
0	Disabled
1	Enabled (Default)

Channel Enable Setting

EN	Setting
0	Disabled
1	Enabled (Default)

MICRO-STAR INT'L CO.,LTD

MS-7D09

Size	Document Description	Rev
Custom	Rear-USB32 GEN2 TYPEA	10

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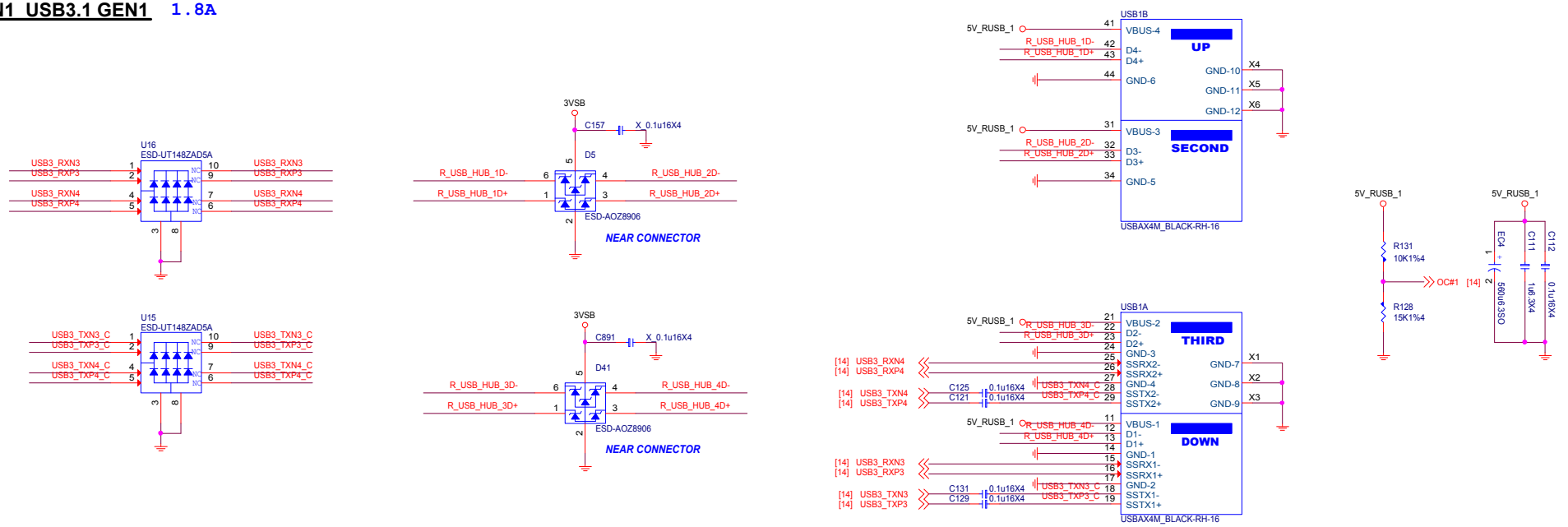
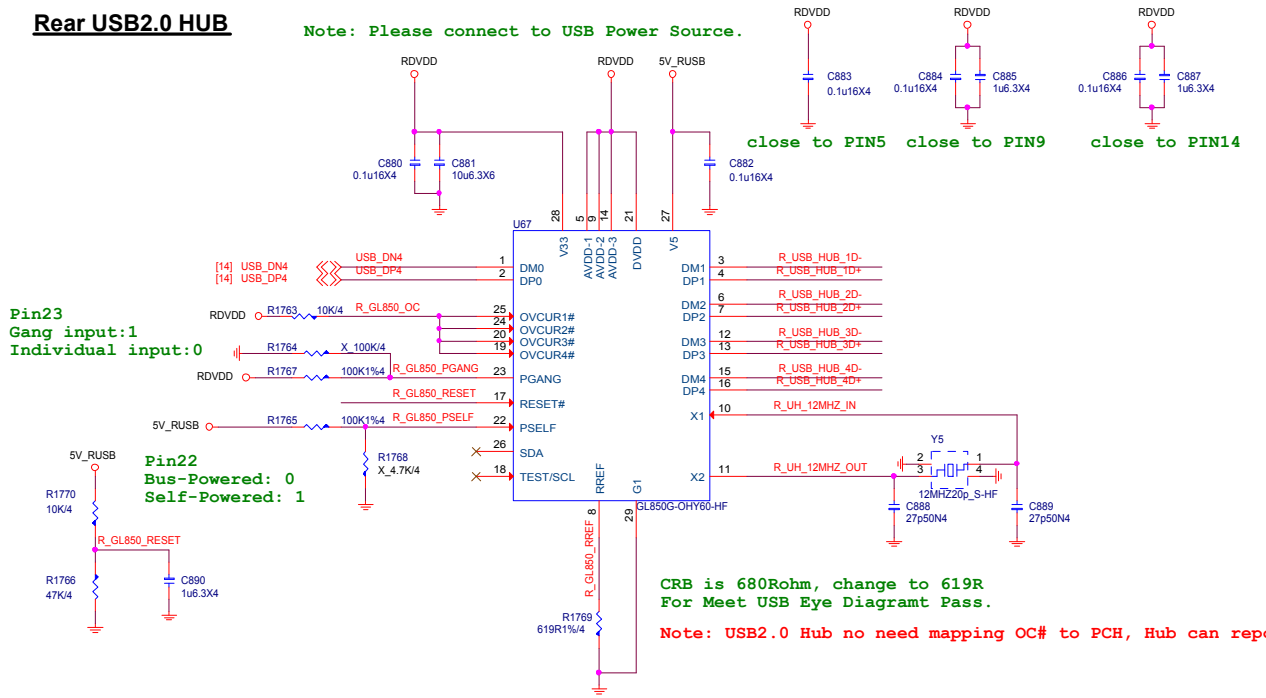
Rear LAN1 USB3.1 GEN1 1.8A



Rear USB2.0 HUB

Note: Please connect to USB Power Source.



CRB is 680Rohm, change to 619R
For Meet USB Eye Diagramt Pass.

Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.

MICRO-STAR INT'L CO.,LTD		
Size: Custom	Document Description: Rear LAN_USB1	Rev
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USB 3.1-Type-C

5 inch< Host to IC < 10 inch

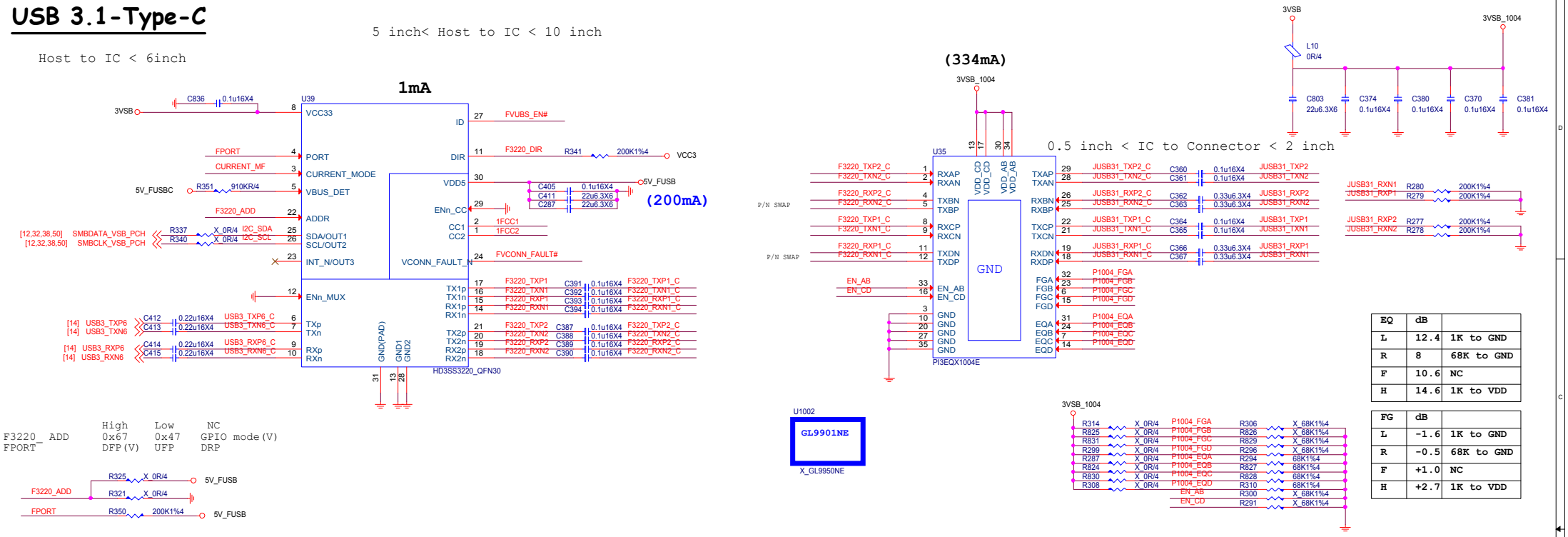
Host to IC < 6inch

1mA

(334mA)

(200mA)

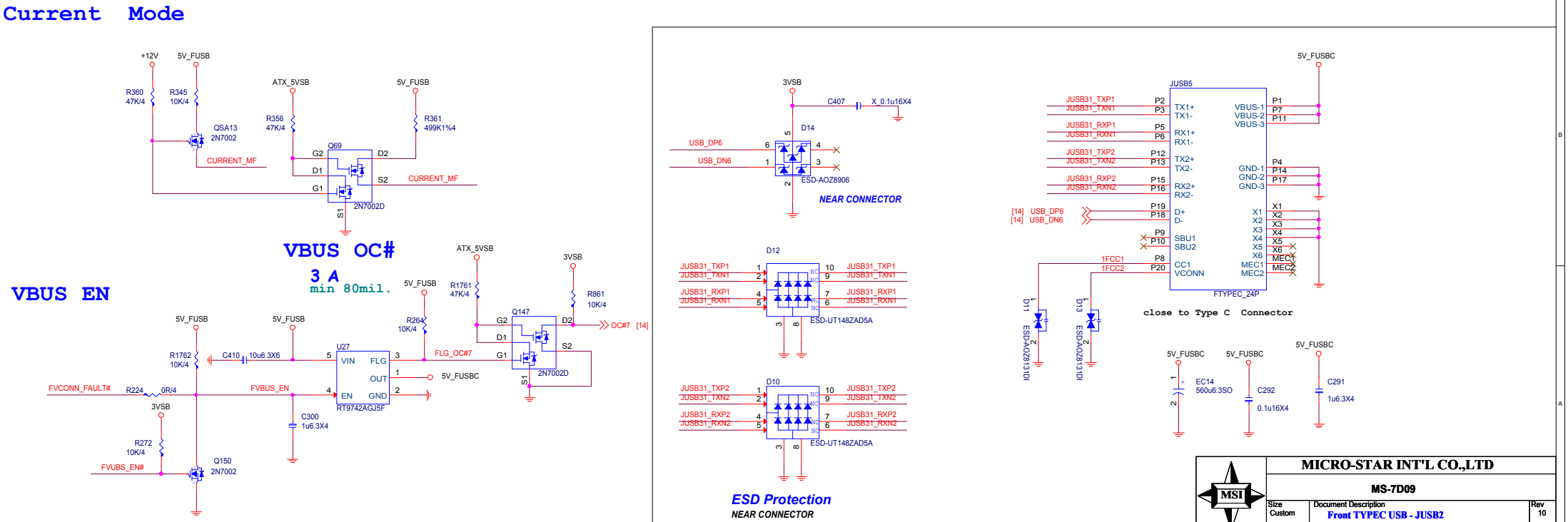
0.5 inch < IC to Connector < 2 inch



EQ	dB	
L	12.4	1K to GND
R	8	68K to GND
F	10.6	NC
H	14.6	1K to VDD

FG	dB	
L	-1.6	1K to GND
R	-0.5	68K to GND
F	+1.0	NC
H	+2.7	1K to VDD

	High	Low	NC
F3220_ ADD	0x67	0x47	GPIO mode(V)
FPORT	DFP(V)	UFP	DRP



MICRO-STAR INT'L CO.,LTD

MS-7D09

Size: Custom | Document Description: Front TYPEC USB - JUSB2 | Rev: 10

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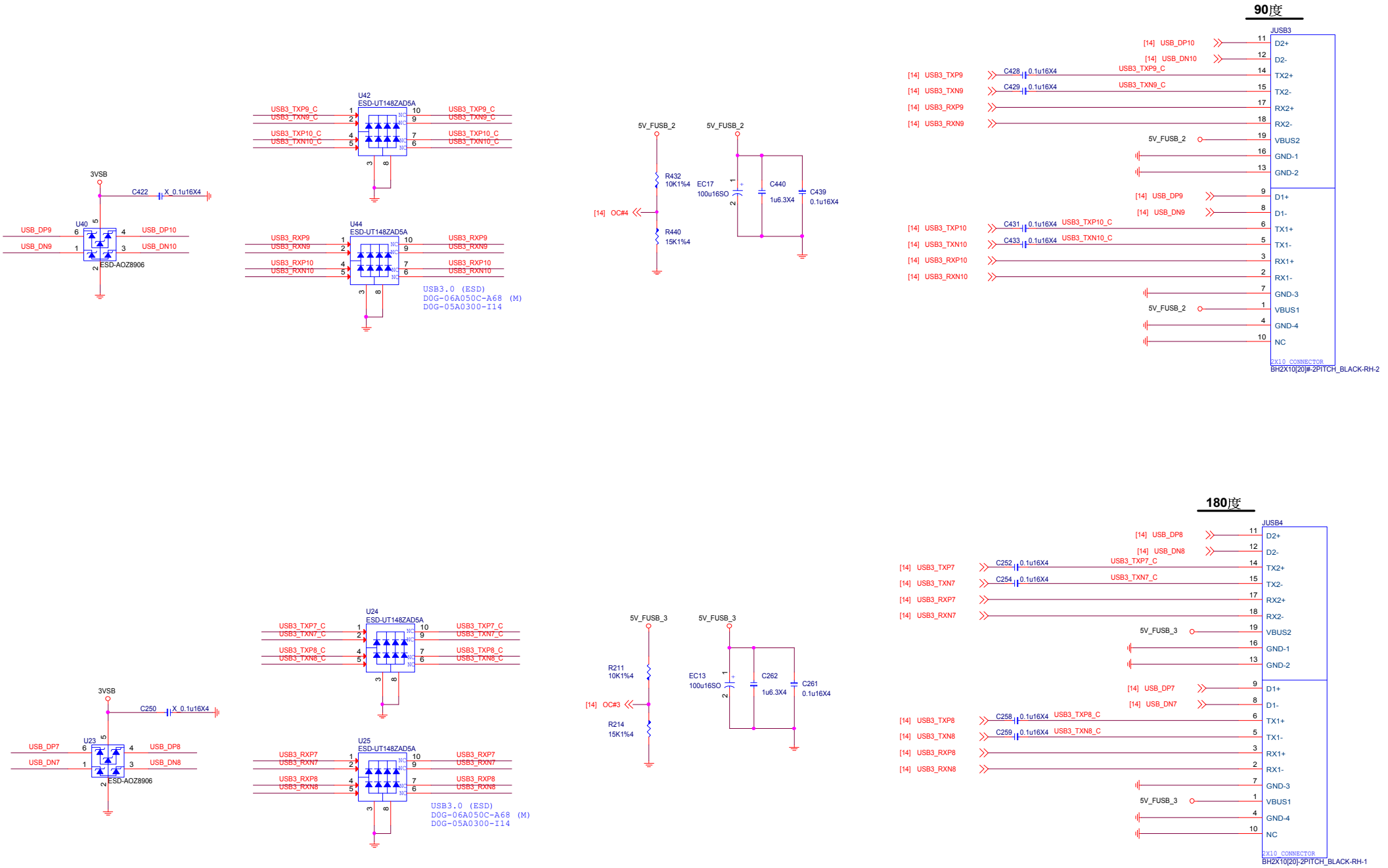

MICRO-STAR INT'L CO.,LTD		
Size Custom	Document Description Front USB30	Rev
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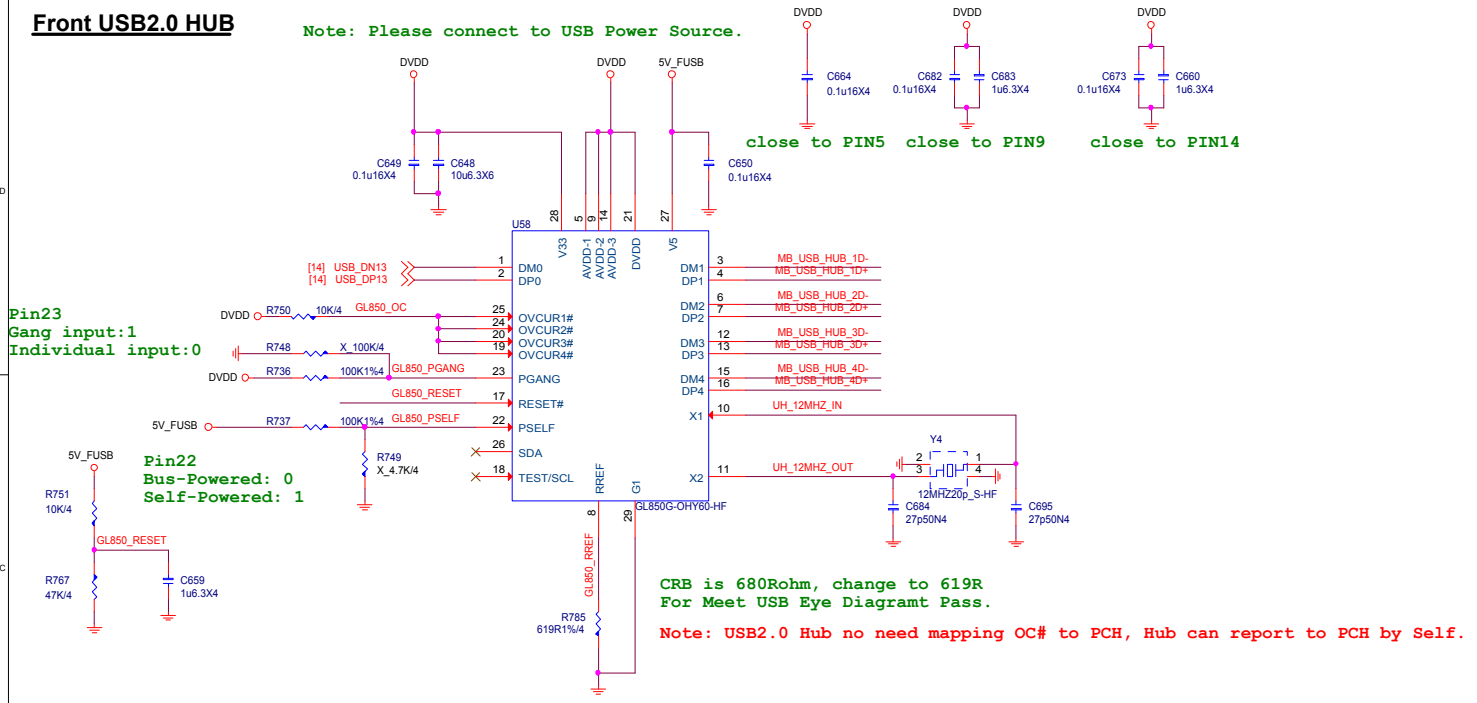
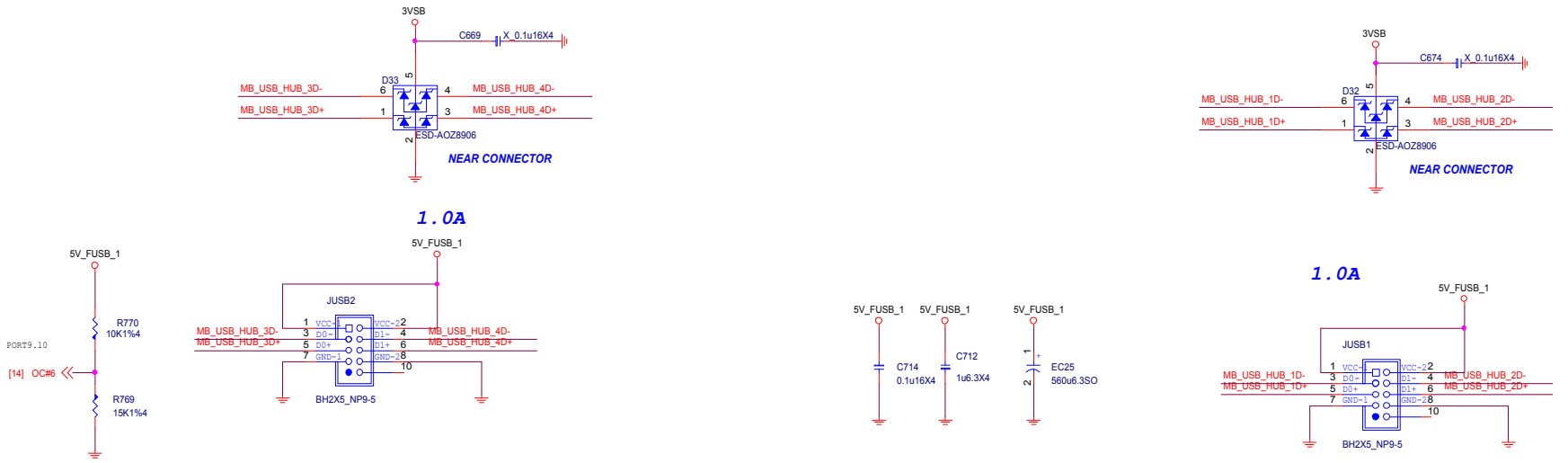
Front USB2.0 HUB

Note: Please connect to USB Power Source.



Rear USB2.0 PORT 9,10



MICRO-STAR INT'L CO.,LTD		
MS-7D09		
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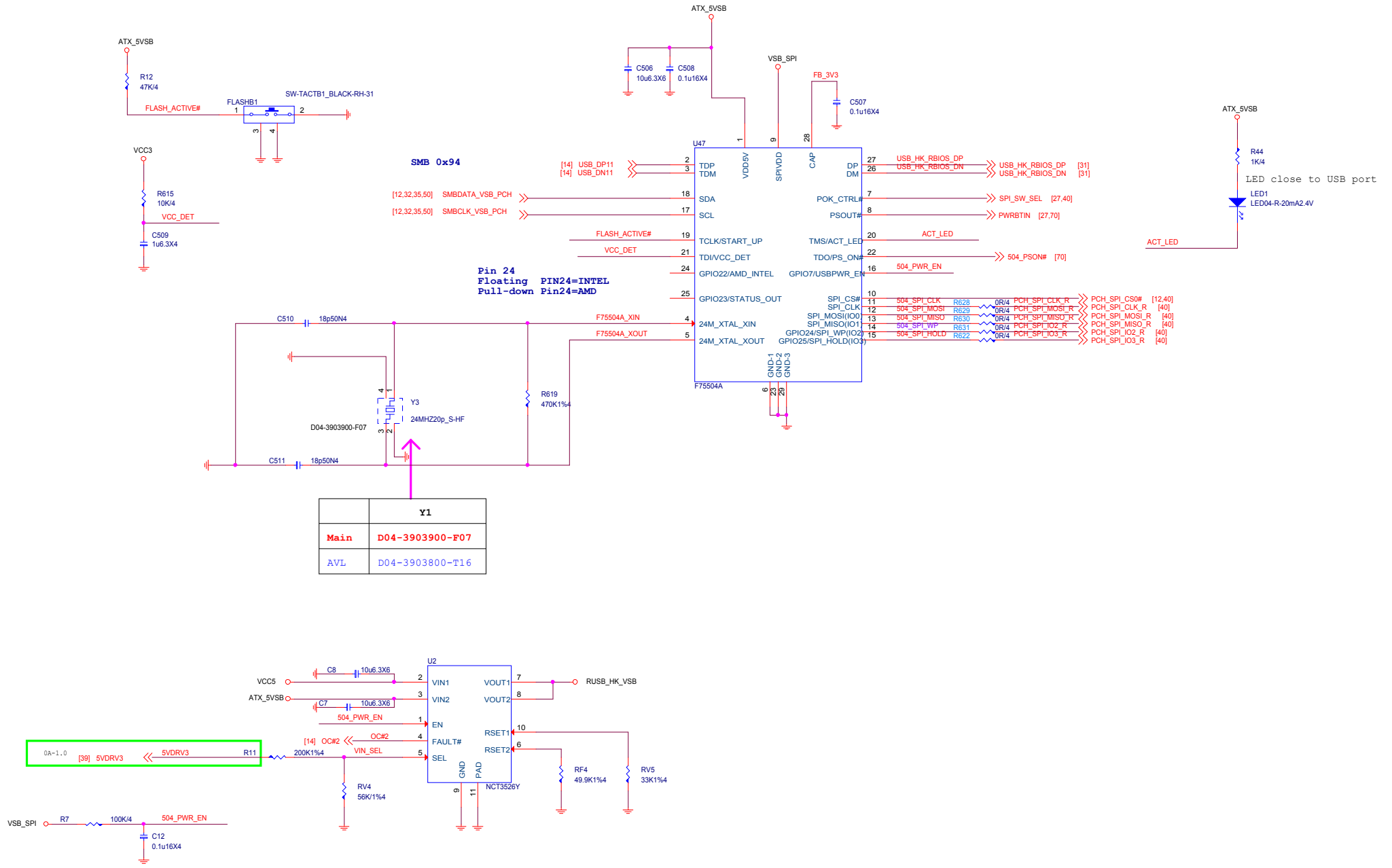
FLASE BIOS



	Y1
Main	D04-3903900-F07
AVL	D04-3903800-T16

MICRO-STAR INT'L CO.,LTD

MS-7D09

Size	Document Description	Rev
Custom	SPI ROM-BIOS	10

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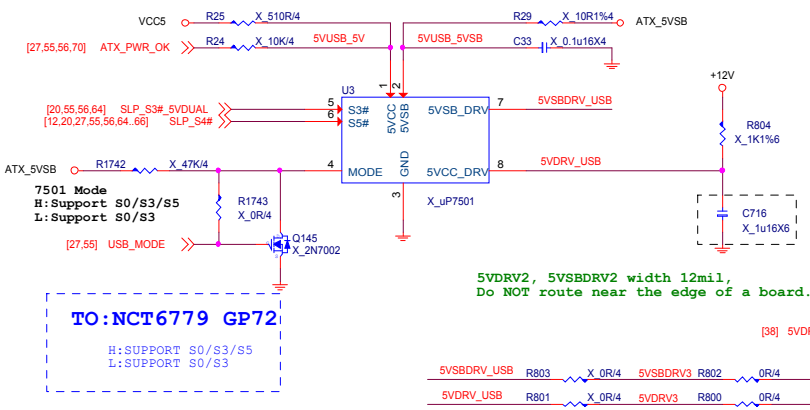
USB POWER

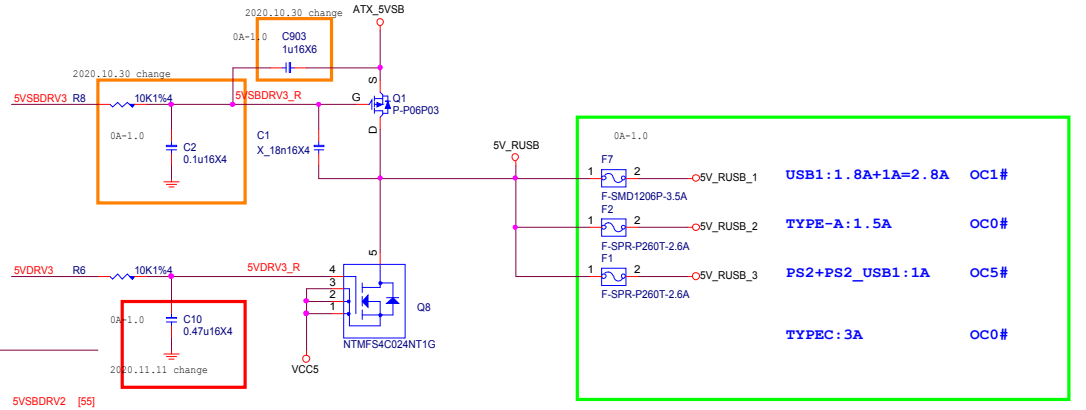


5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

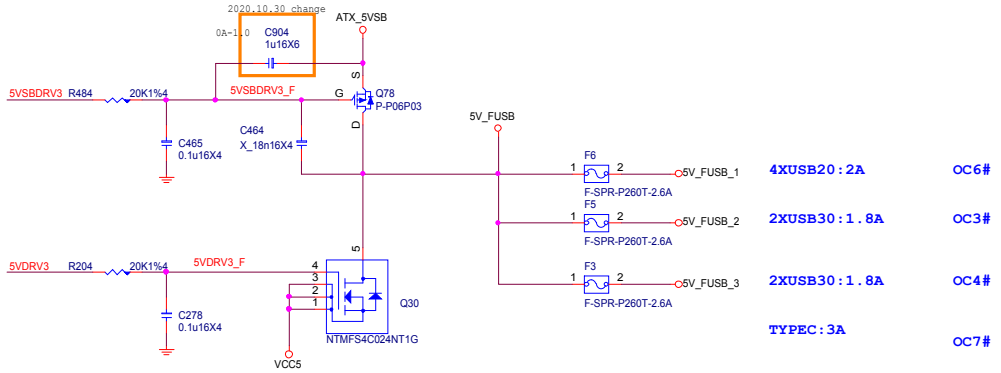
5VSBDRV_USB R803 X_0R/4 5VSBDRV3 R802 0R/4 5VSBDRV2 — 5VSBDRV2 [55]

5VDRV_USB R801 X_0R/4 5VDRV3 R800 0R/4 5VDRV2 — 5VDRV2 [55]

REAR USB PORT POWER



FRONT USB PORT POWER



MICRO-STAR INT'L CO.,LTD		
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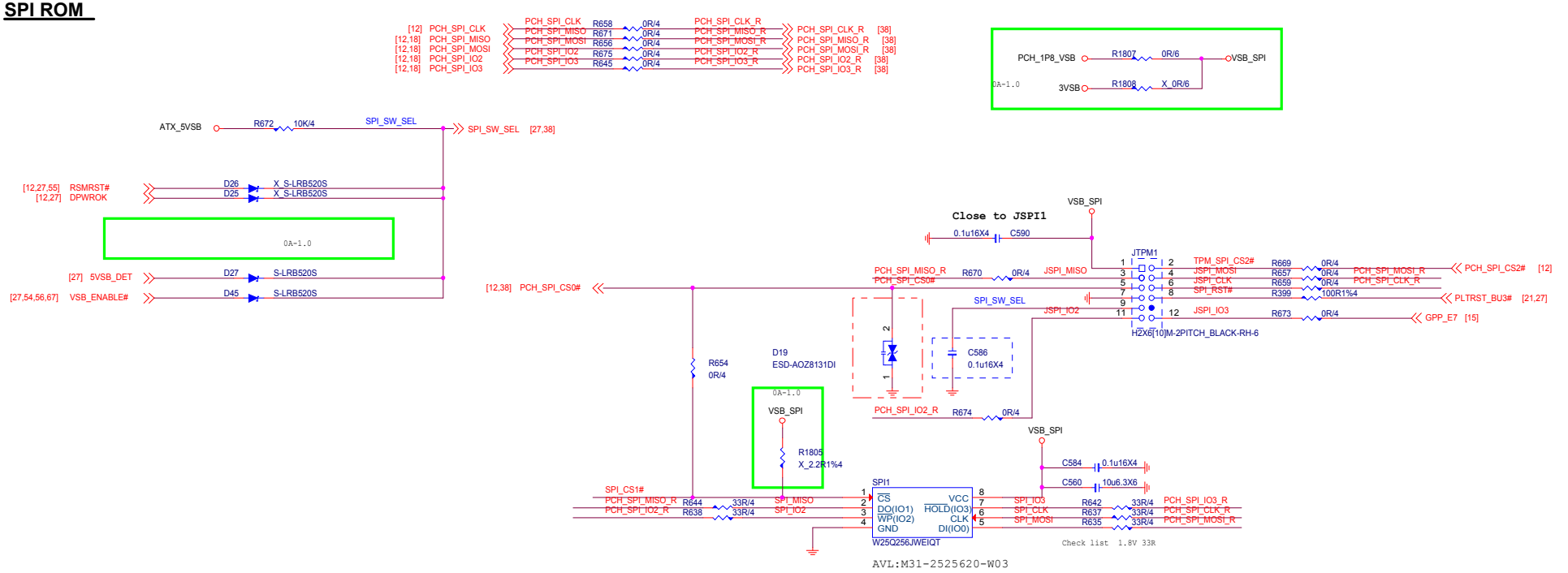
SPI ROM



MICRO-STAR INT'L CO.,LTD			
MS-7D09			
Size: Custom	Document Description: SPI ROM		Rev: 10
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1.For non-vPro platforms or standard PCIe device: SMBUS is not required (2.2K-10K pull-ups to +3.3V_LAN).
2.For vPRO platforms: I225 SMBUS must connect to PCH's SMLINK0
3.The pull-up power rail should be same with PCH's SMLINK0 power rail (to avoid leakge current)

Intel I225V

SMBUS Addess 0x49

UL1 — I225

PCIE: PE_TX_P, PE_TX_N, PE_RX_P, PE_RX_N, PE_CLK_P, PE_CLK_N, PE_CLKREQ_N, PE_WAKE_N, PE_RST_N
MDI: MDI_A_P, MDI_A_N, MDI_B_P, MDI_B_N, MDI_C_P, MDI_C_N, MDI_D_P, MDI_D_N
SMBUS: SMB_CLK, SMB_DATA, ULP_WAKE_N
LED: LED0, LED1, LED2
POWER: LAN_PWR_GOOD, LAN_DISABLE_N, SDP0, RBIAS, PHY_CAL; +3.3V_PAD-1, +3.3V_PAD-2, +3.3V_DC, +3.3V_VPH, +3.3V_XO, +3.3V_CDB, +3V3_A-1, +3V3_A-2, VDD_CTRL-1, VDD_CTRL-2, VDD_VP, VDD_CORE-1, VDD_CORE-2, VDD_A-1, VDD_A-2, VDD_A-3, RESERVED, EPAD
SPI: SPI_DOUT/SEC_ENA, SPI_CLK, SPI_DIN/AUX_PWR, SPI_CS_N/PCIE_ENA
JTAG: JTAG_RST, JTAG_TMS_SDP2, JTAG_TDO/MDI_LANE_SWAP, JTAG_TDI_SDP1, JTAG_CLK
CRYSTAL: XTAL_OUT, XTAL_IN

SMBUS PULL-UP OPTIONS
SMBUS SPEED
1MHz (Defaul setting) 499 ohm
100KHz/400KHz 2.2K ohm

check CLKREQ pull up in PCH Side

LAN_DISABLE_N Pin:
Connect LAN_Disable_N(2) to PCH's LANPHYPC pin.
If this pin is already used for I219, connect to PCH's GPIO.
*If not use: Pull up LAN_DISABLE_N(2) with a 10 Kohm resistor to 3.3V.

0.1uF PER PIN

CHOKEL1:L04-01073M0-M26
AVL:EP-10AM04T04
WIP201610S-1R0ML

700mA

2020.10.30 change 18p

For EMI

Co-lay 8PIN TVS
need change UPI PN

UL3&UL5 close to connector

Main:D0G-06A030C-A68
AVL:Follow LOB AVL

RL28
PCIe Disable Strapping
(Normal Operation: Empty)

Optional Security Strapping
Short JL1 to disable Flash Security
Normal Operation: No Jumper

190829:Add I225_SPI_CLK 10K to GND

+3.3V_LAN

I225:?

MICRO-STAR INT'L CO.,LTD

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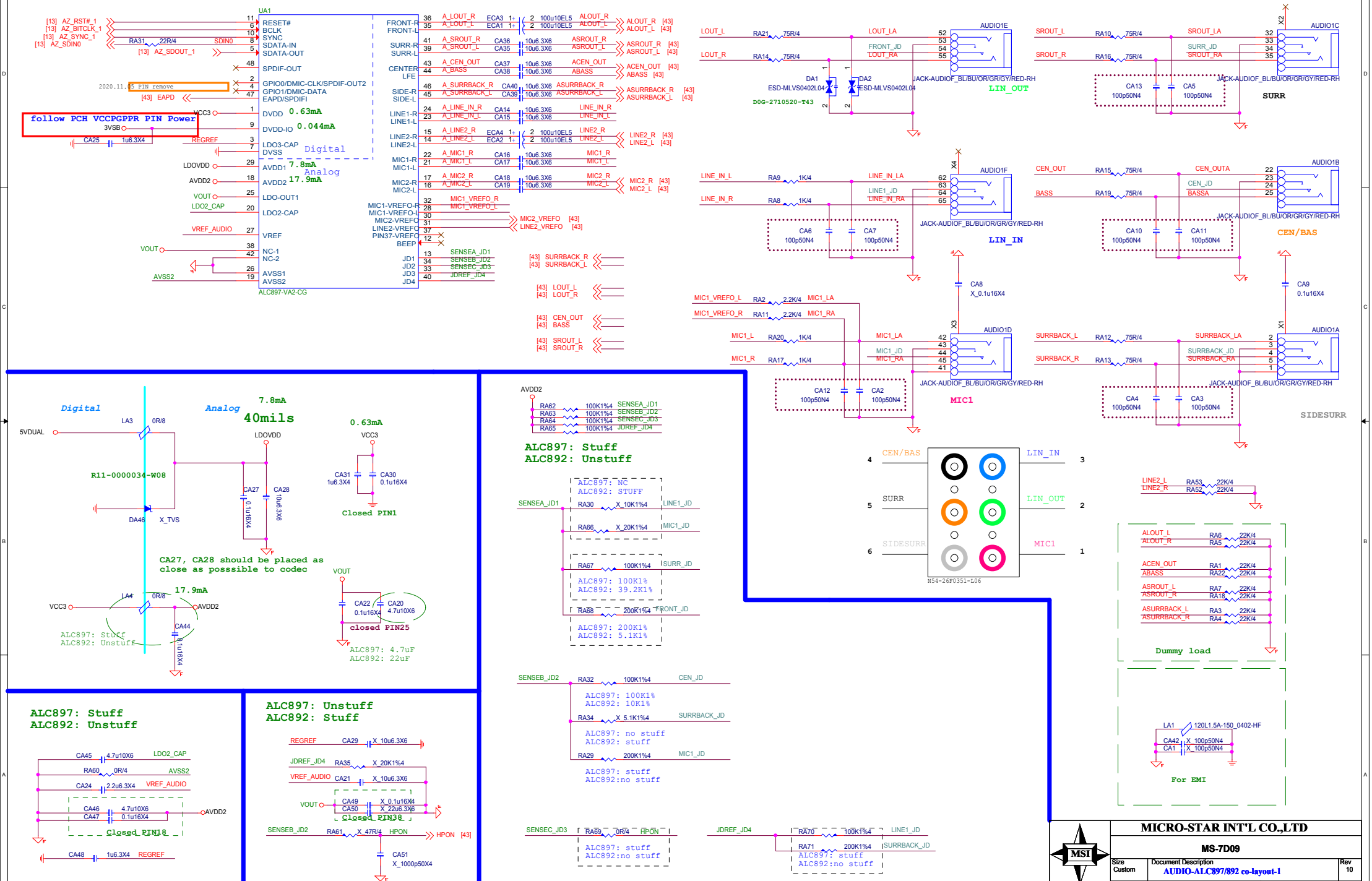
ALC897


UA1
ALC897-VA2-CG
follow PCH VCCPGPPR PIN Power
2020.11.5 PIN remove
Digital
Analog
0.63mA
0.044mA
7.8mA
17.9mA
LIN_OUT
SURR
LIN_IN
CEN/BAS
MIC1
SIDESURR
JACK-AUDIOF_BL/BU/OR/GR/GY/RED-RH
ALC897: Stuff
ALC892: Unstuff
ALC897: Unstuff
ALC892: Stuff
Closed PIN1
Closed PIN25
Closed PIN18
Closed PIN38
CA27, CA28 should be placed as close as posssible to codec
ALC897: 4.7uF
ALC892: 22uF
Dummy load
For EMI
MICRO-STAR INT'L CO.,LTD
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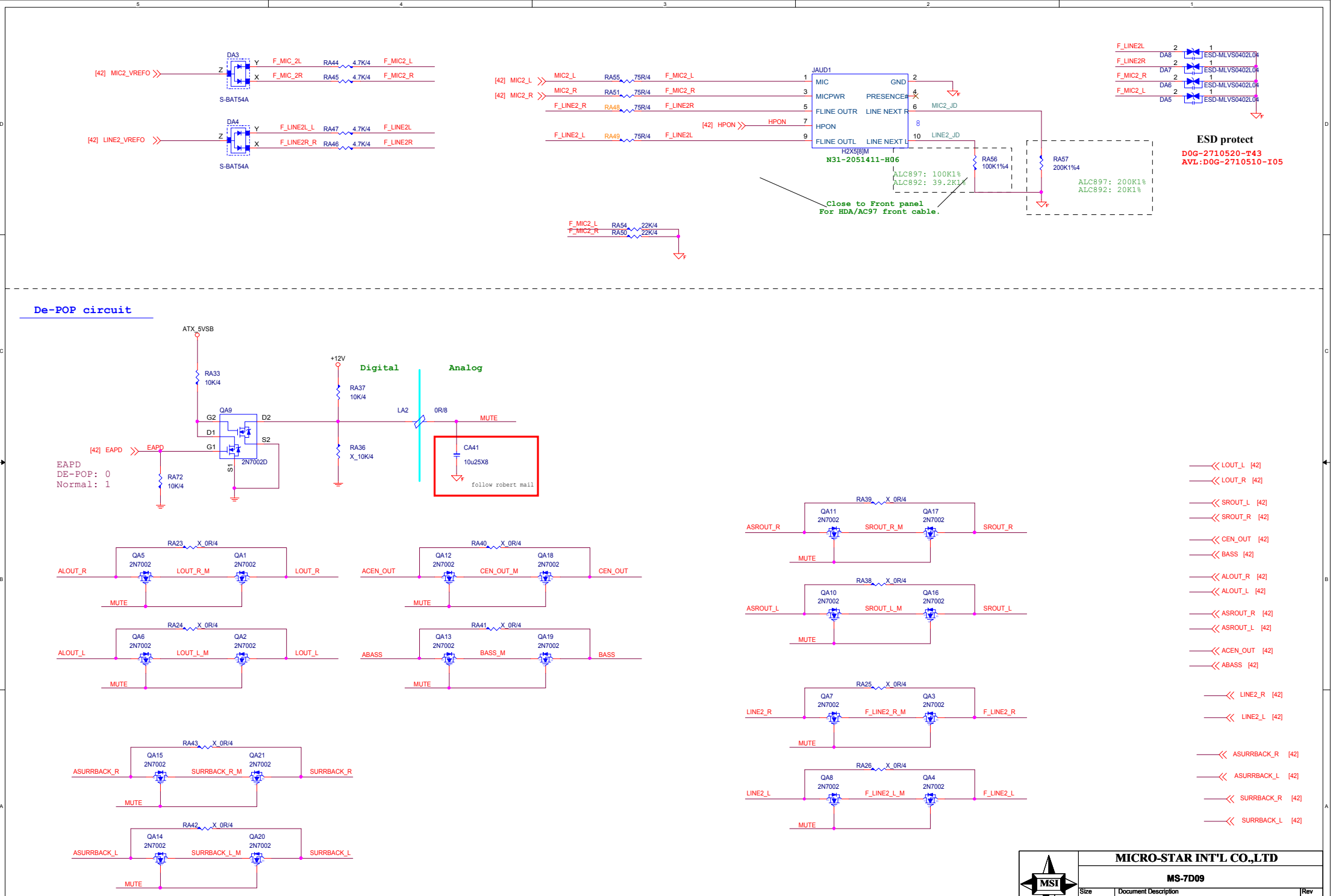
DA3
S-BAT54A
[42] MIC2_VREFO
F_MIC_2L
F_MIC_2R
RA44 4.7K/4
RA45 4.7K/4
F_MIC2_L
F_MIC2_R
DA4
S-BAT54A
[42] LINE2_VREFO
F_LINE2L_L
F_LINE2R_R
RA47 4.7K/4
RA46 4.7K/4
F_LINE2L
F_LINE2R
JAUD1
MIC
MICPWR
FLINE OUTR
HPON
FLINE OUTL
GND
PRESENCE#
LINE NEXT R
LINE NEXT L
H2X5[8]M
N31-2051411-H06
[42] MIC2_L
[42] MIC2_R
MIC2_L RA55 75R/4 F_MIC2_L
MIC2_R RA51 75R/4 F_MIC2_R
F_LINE2_R RA48 75R/4 F_LINE2R
F_LINE2_L RA49 75R/4 F_LINE2L
[42] HPON
HPON
MIC2_JD
LINE2_JD
RA56 100K1%4
RA57 200K1%4
ALC897: 100K1%
ALC892: 39.2K1%
ALC897: 200K1%
ALC892: 20K1%
Close to Front panel
For HDA/AC97 front cable.
F_MIC2_L RA54 22K/4
F_MIC2_R RA50 22K/4
F_LINE2L DA8 ESD-MLVS0402L04
F_LINE2R DA7 ESD-MLVS0402L04
F_MIC2_R DA6 ESD-MLVS0402L04
F_MIC2_L DA5 ESD-MLVS0402L04
ESD protect
D0G-2710520-T43
AVL:D0G-2710510-I05
De-POP circuit
ATX_5VSB
RA33 10K/4
+12V
RA37 10K/4
Digital
Analog
QA9
G2
D1
G1
D2
S2
S1
2N7002D
[42] EAPD
EAPD
RA72 10K/4
RA36 X_10K/4
LA2
0R/8
MUTE
CA41 10u25X8
follow robert mail
EAPD
DE-POP: 0
Normal: 1
RA23 X_0R/4
QA5 2N7002
QA1 2N7002
ALOUT_R
LOUT_R_M
LOUT_R
RA24 X_0R/4
QA6 2N7002
QA2 2N7002
ALOUT_L
LOUT_L_M
LOUT_L
RA40 X_0R/4
QA12 2N7002
QA18 2N7002
ACEN_OUT
CEN_OUT_M
CEN_OUT
RA41 X_0R/4
QA13 2N7002
QA19 2N7002
ABASS
BASS_M
BASS
RA43 X_0R/4
QA15 2N7002
QA21 2N7002
ASURRBACK_R
SURRBACK_R_M
SURRBACK_R
RA42 X_0R/4
QA14 2N7002
QA20 2N7002
ASURRBACK_L
SURRBACK_L_M
SURRBACK_L
RA39 X_0R/4
QA11 2N7002
QA17 2N7002
ASROUT_R
SROUT_R_M
SROUT_R
RA38 X_0R/4
QA10 2N7002
QA16 2N7002
ASROUT_L
SROUT_L_M
SROUT_L
RA25 X_0R/4
QA7 2N7002
QA3 2N7002
LINE2_R
F_LINE2_R_M
F_LINE2_R
RA26 X_0R/4
QA8 2N7002
QA4 2N7002
LINE2_L
F_LINE2_L_M
F_LINE2_L
LOUT_L [42]
LOUT_R [42]
SROUT_L [42]
SROUT_R [42]
CEN_OUT [42]
BASS [42]
ALOUT_R [42]
ALOUT_L [42]
ASROUT_R [42]
ASROUT_L [42]
ACEN_OUT [42]
ABASS [42]
LINE2_R [42]
LINE2_L [42]
ASURRBACK_R [42]
ASURRBACK_L [42]
SURRBACK_R [42]
SURRBACK_L [42]
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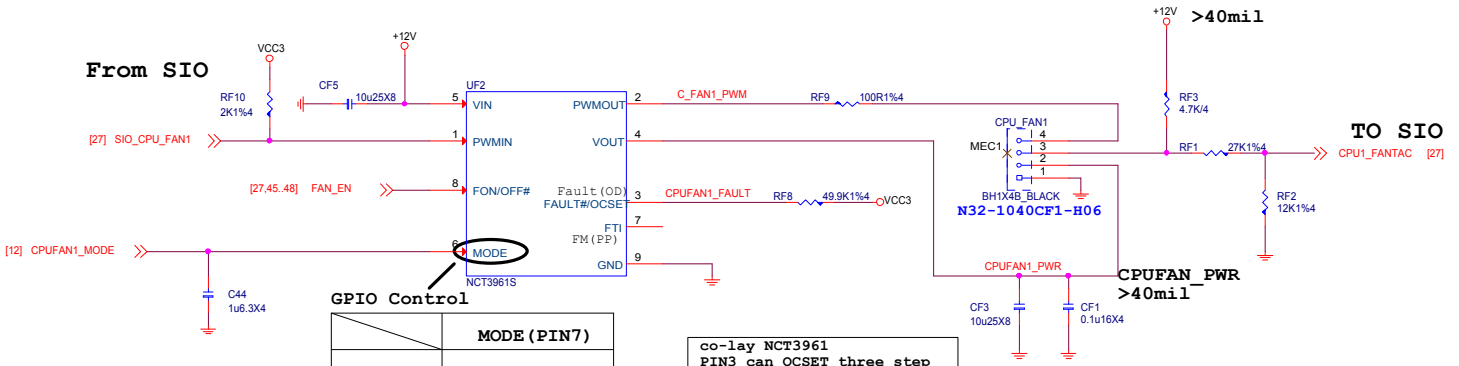
TYPE M:CPU FAN



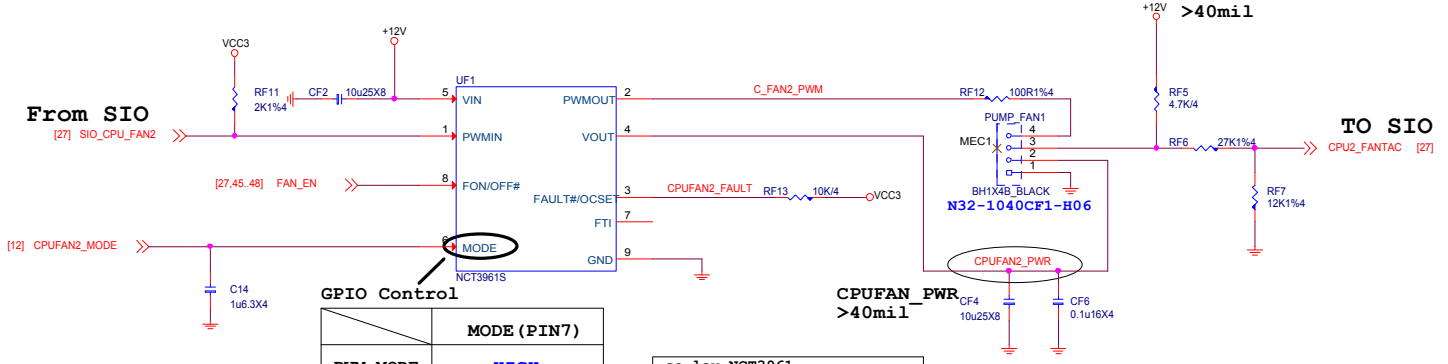
GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

co-lay NCT3961
PIN3 can OCSET three step
10K=3.2~3.8A
49.9K=2.2~2.8A
100K=1.2~1.8A

OC SET By PM SPEC

TYPE M : PUMP FAN



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

co-lay NCT3961
PIN3 can OCSET three step
10K=3.2~3.8A
49.9K=2.2~2.8A
100K=1.2~1.8A

OC SET By PM SPEC

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	MS-7D09	
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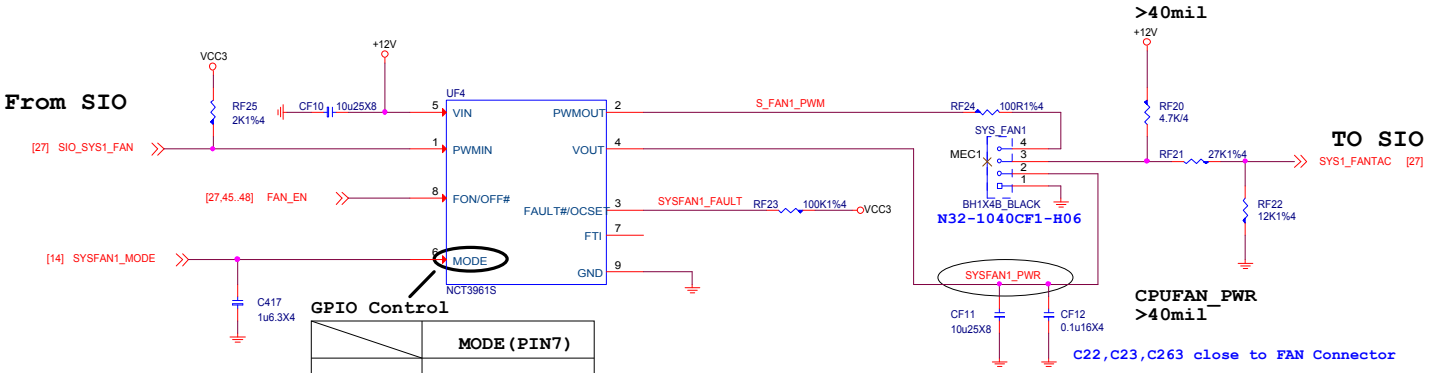
TYPE M : SYSTEM FAN1

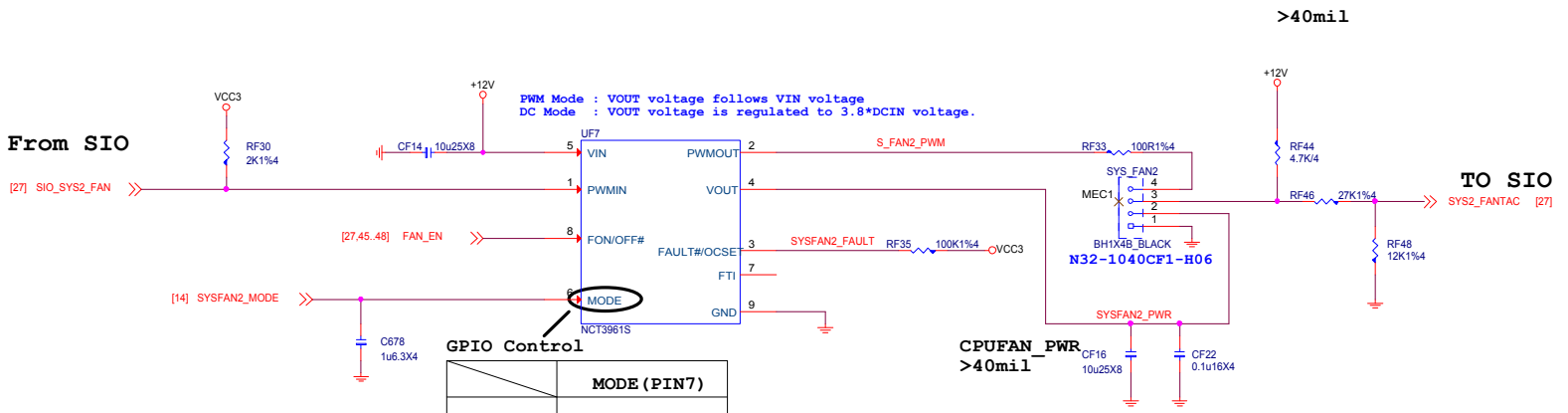


GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

TYPE M :SYSTEM FAN2



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D09	
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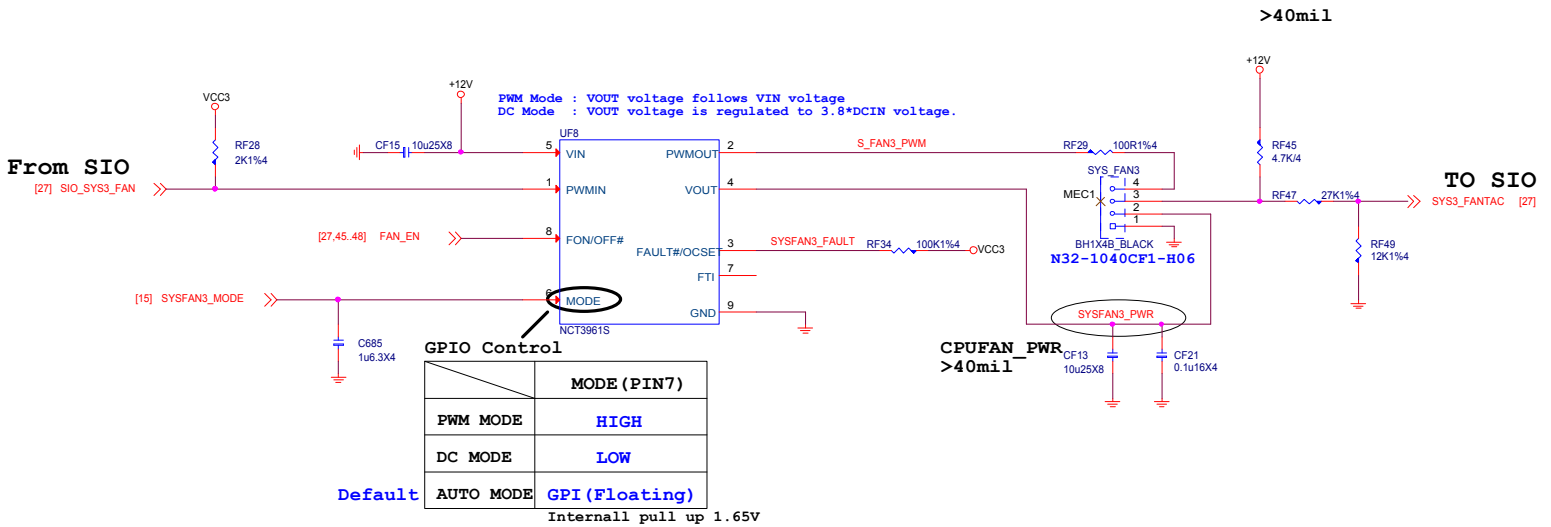
TYPE M : SYSTEM FAN3

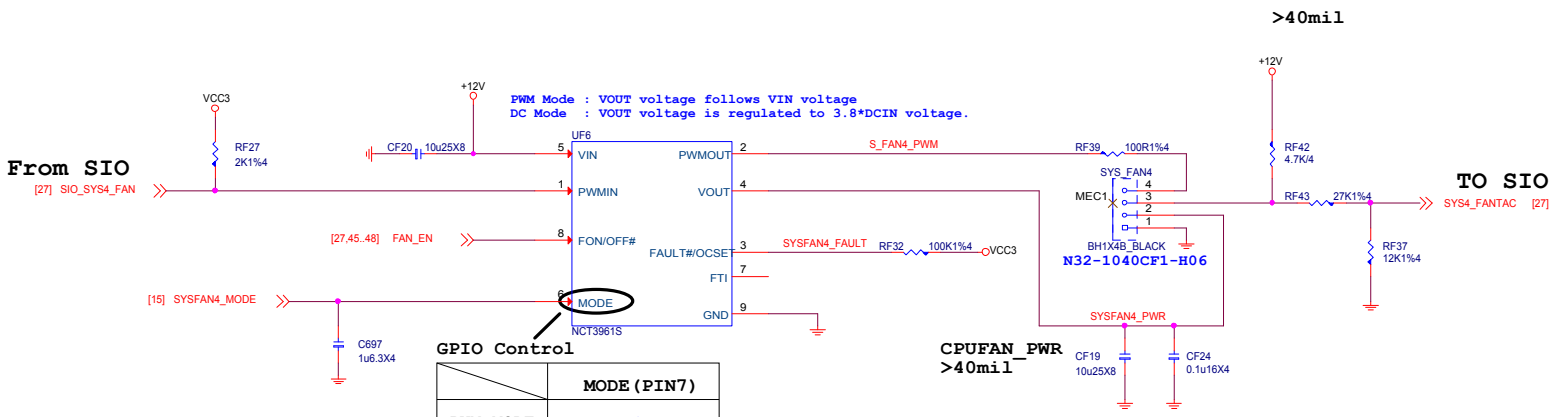


GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

TYPE M :SYSTEM FAN4



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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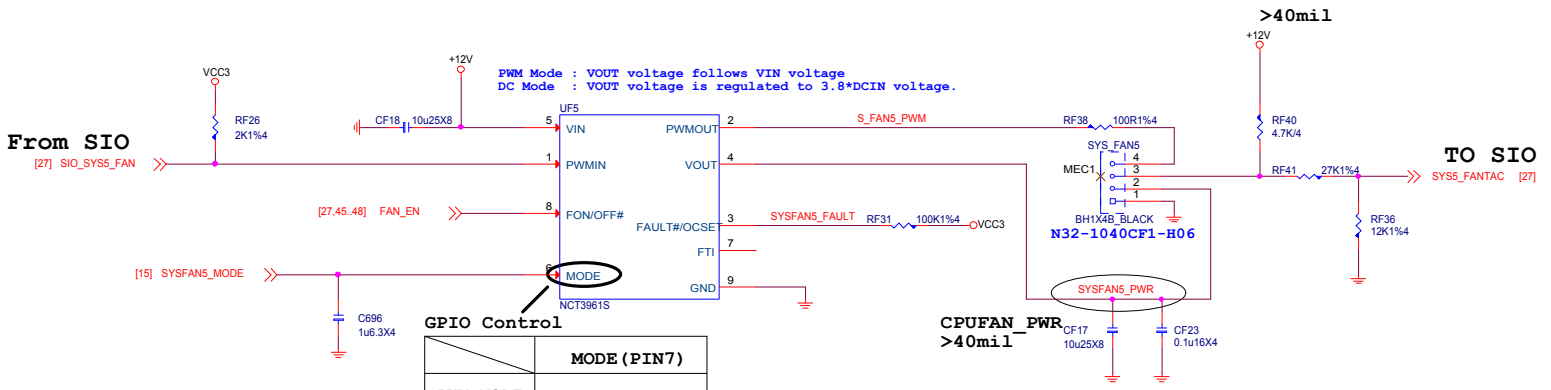
TYPE M : SYSTEM FAN5

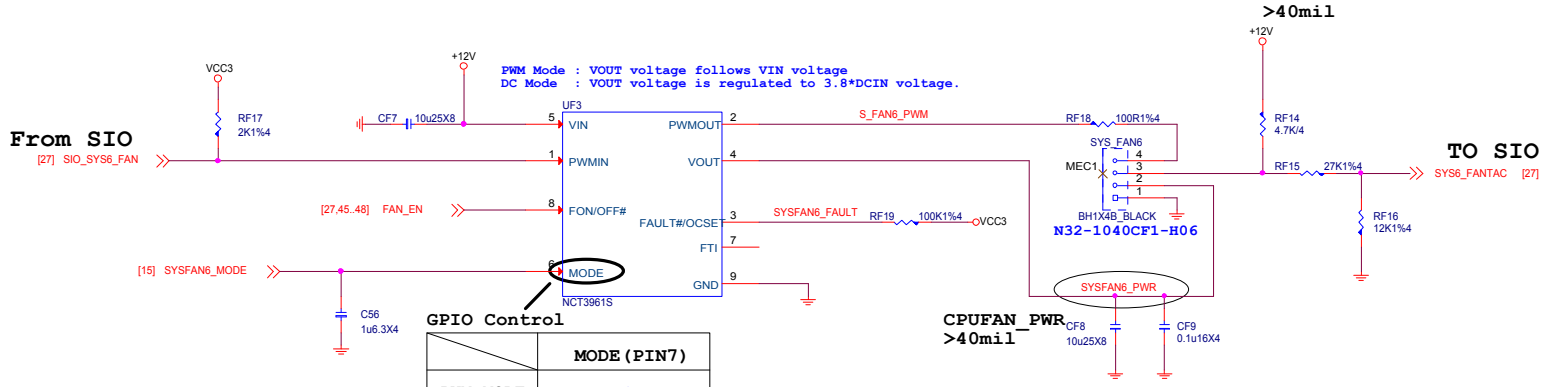


GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

TYPE M : SYSTEM FAN6



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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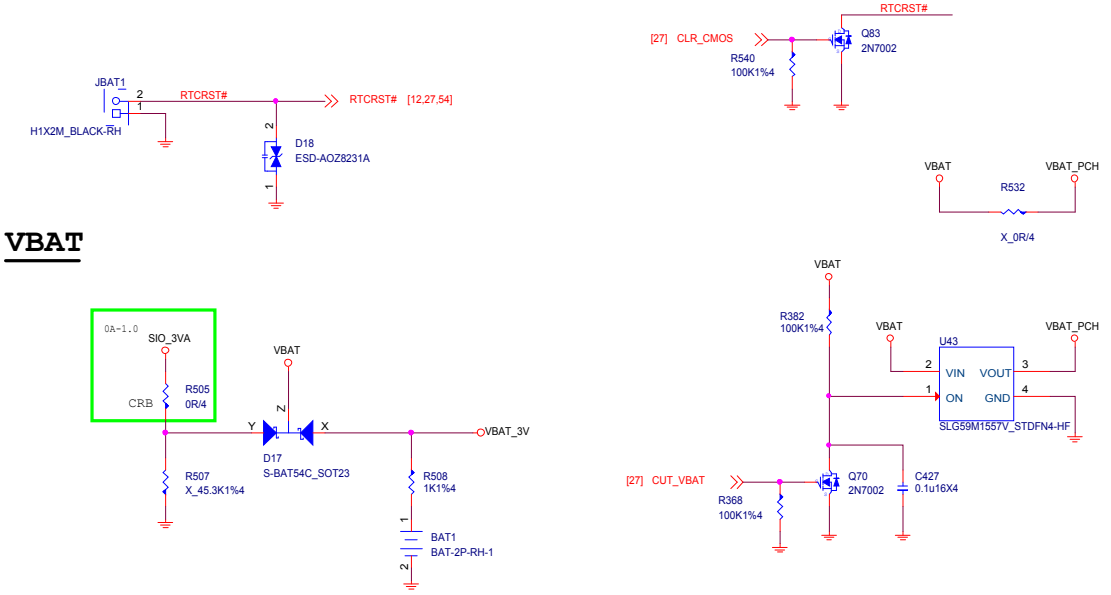
CLR COMS



VBAT

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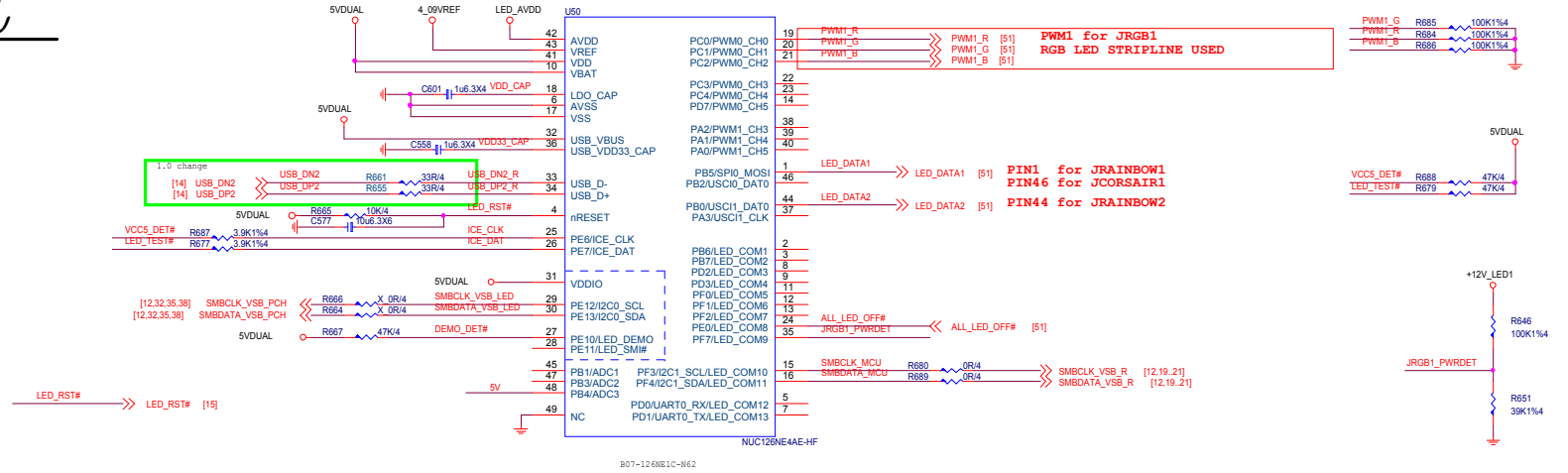
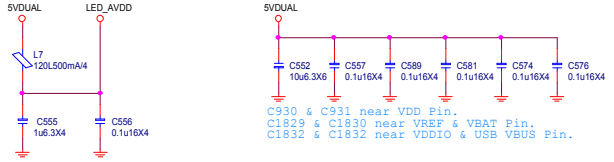
LED MCU

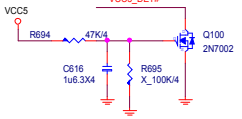


Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~16	PWM2

C1811 & C1812 near AVDD Pin.



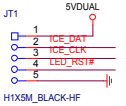
C930 & C931 near VDD Pin.
C1829 & C1830 near VREF & VBAT Pin.
C1832 & C1832 near VDDIO & USB VBUS Pin.



IF no JPWRLED1 & JPIPE_LED spec

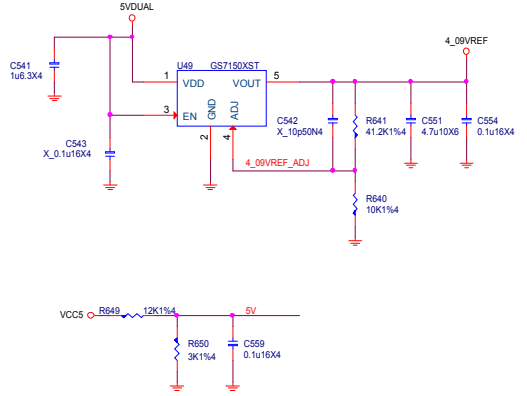
MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

For FW update.



0A-1.0 Remove JF1

MCU Voltage Monitor



MICRO-STAR INT'L CO.,LTD

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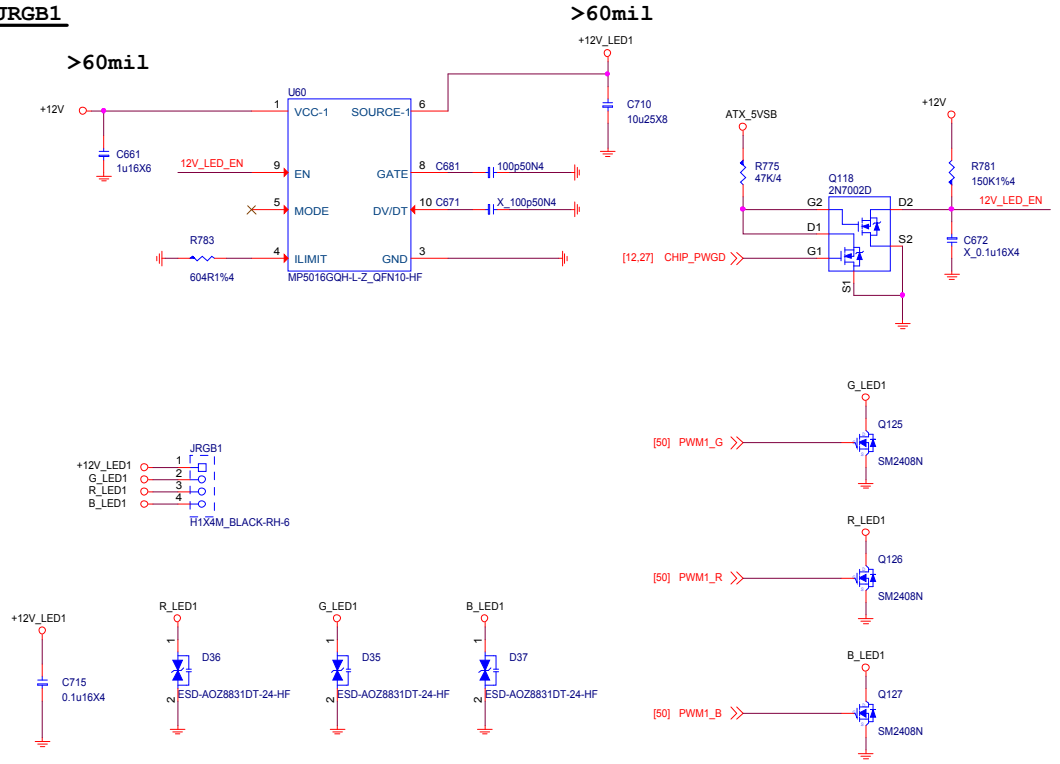
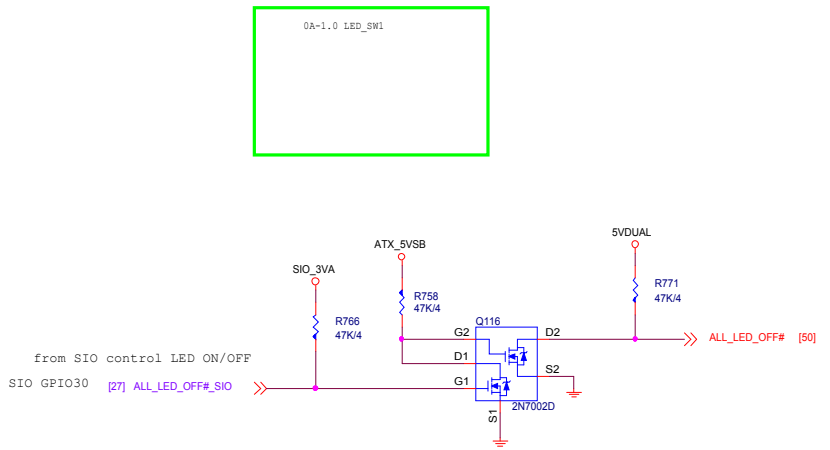
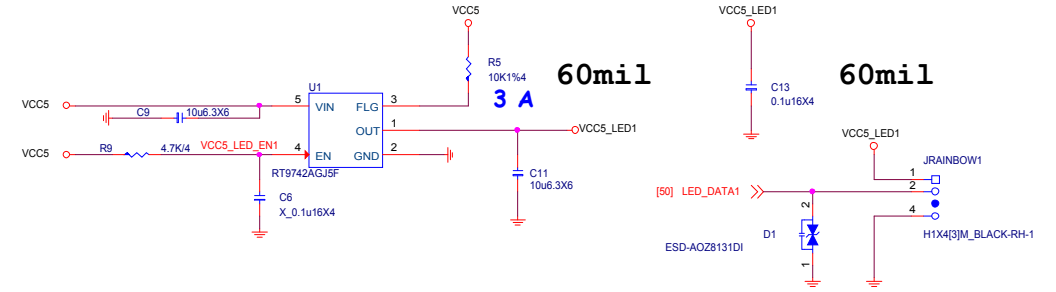
JRGB1



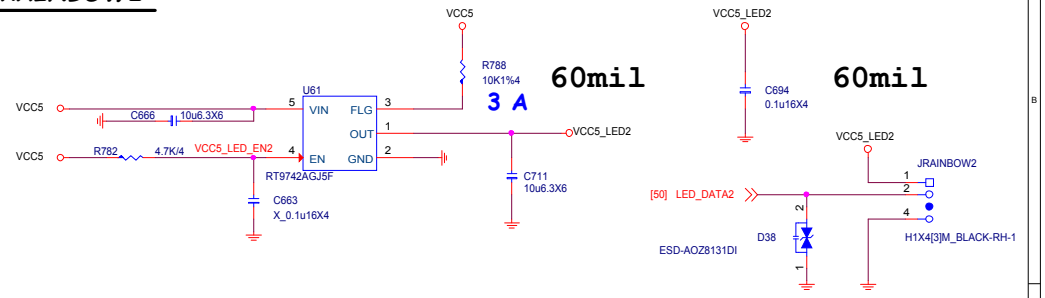
ALL LED OFF#



JRAINBOW1



JRAINBOW2



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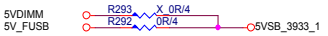
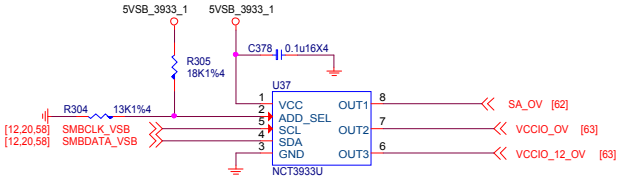


UPI VOLTAGE CONSOLE

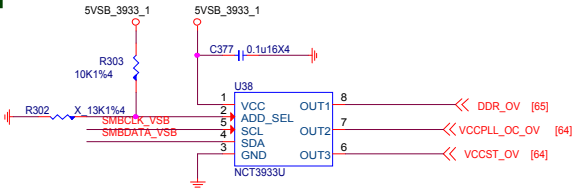
0x26:RH=18K,RL=13K



ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

UPI VOLTAGE CONSOLE

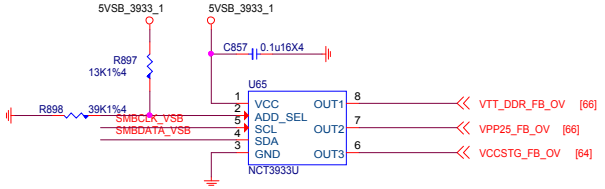
0x20:RH=10K,RL=OPEN



UPI VOLTAGE CONSOLE

0A-1.0

0x22:RH=13,RL=39K



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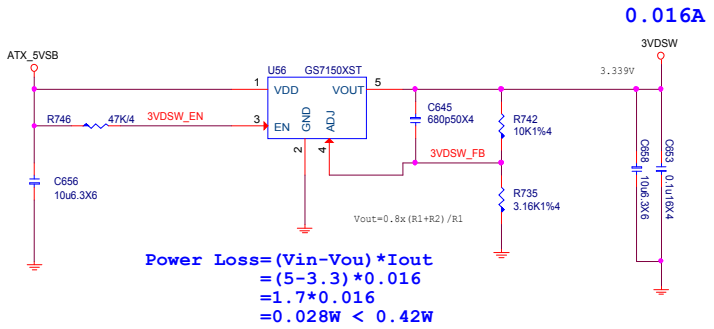
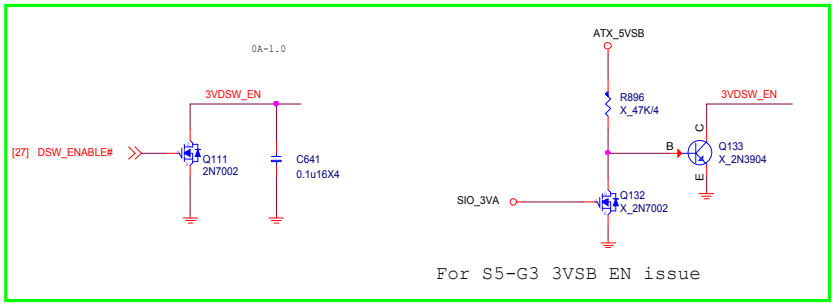
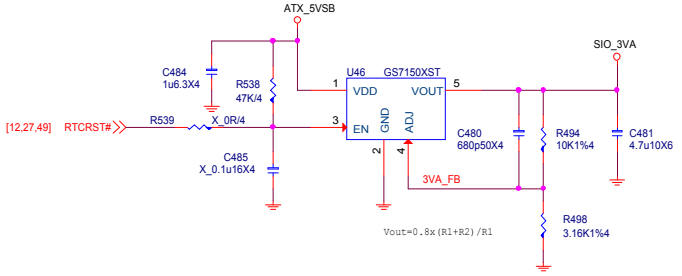
3VDSW

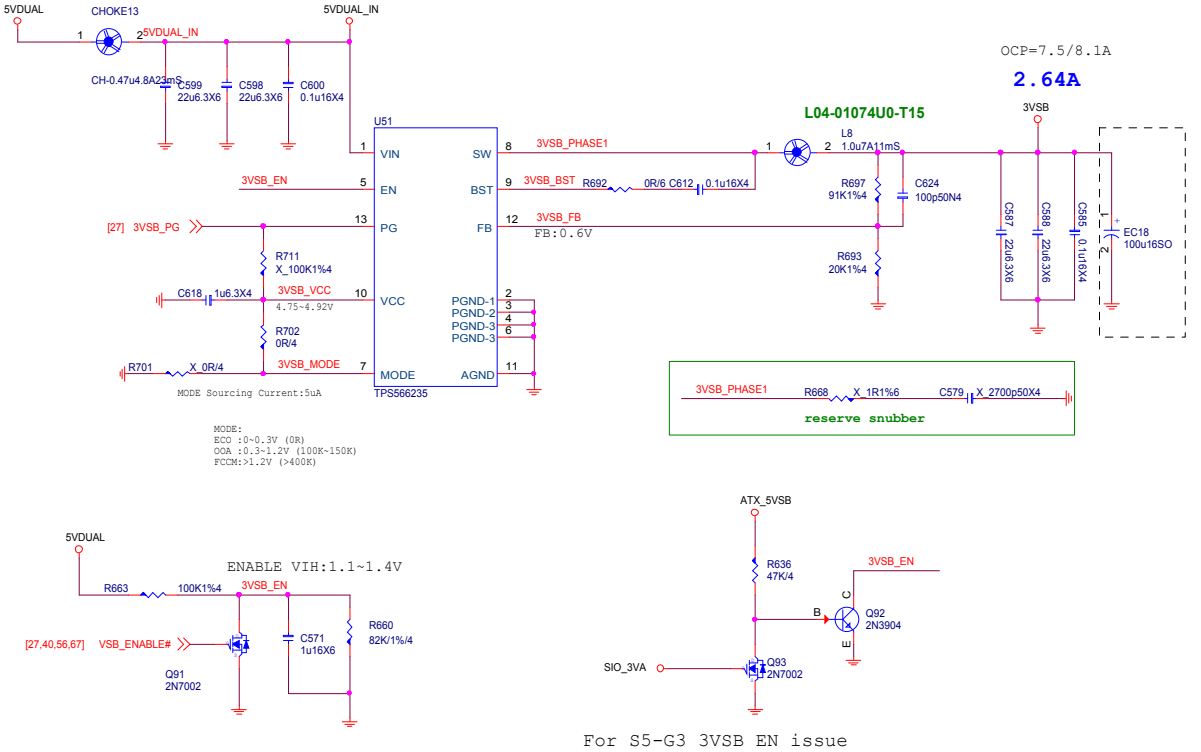




SIO_3VA



SYS_3VSB



For S5-G3 3VSB EN issue

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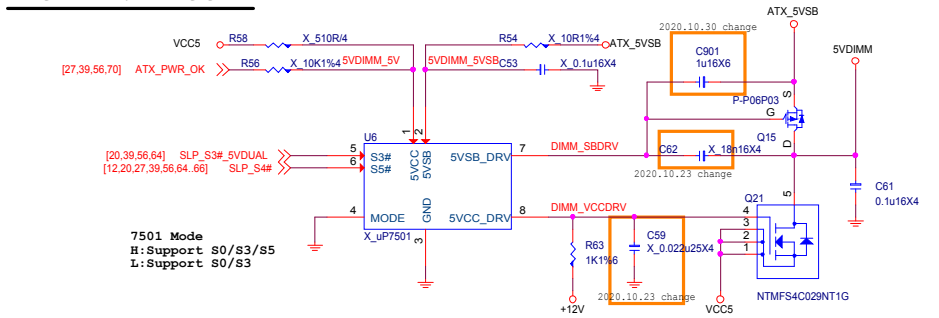
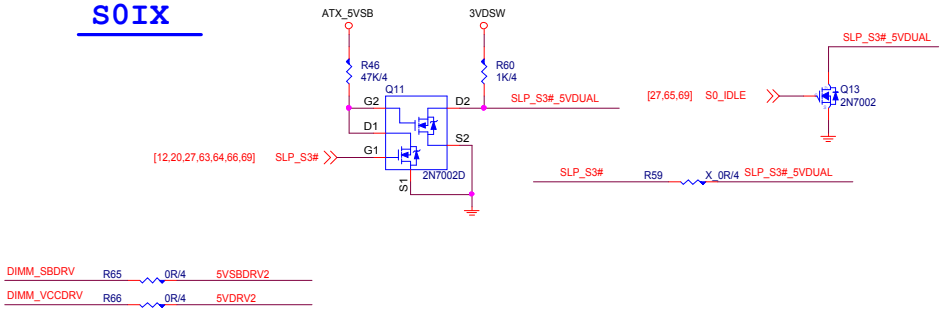
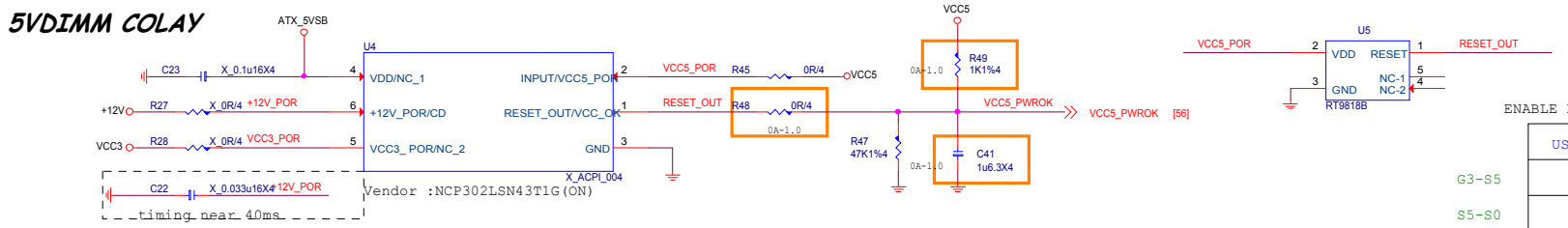
5VDIMM FOR DDR



S0IX



5VDIMM COLAY



PIN6 CAP for fine tune RESET_OUT dealy time use
When INPUT rising up to 4.3V(Vth) level besides delay 35ms~40ms send Reset Output

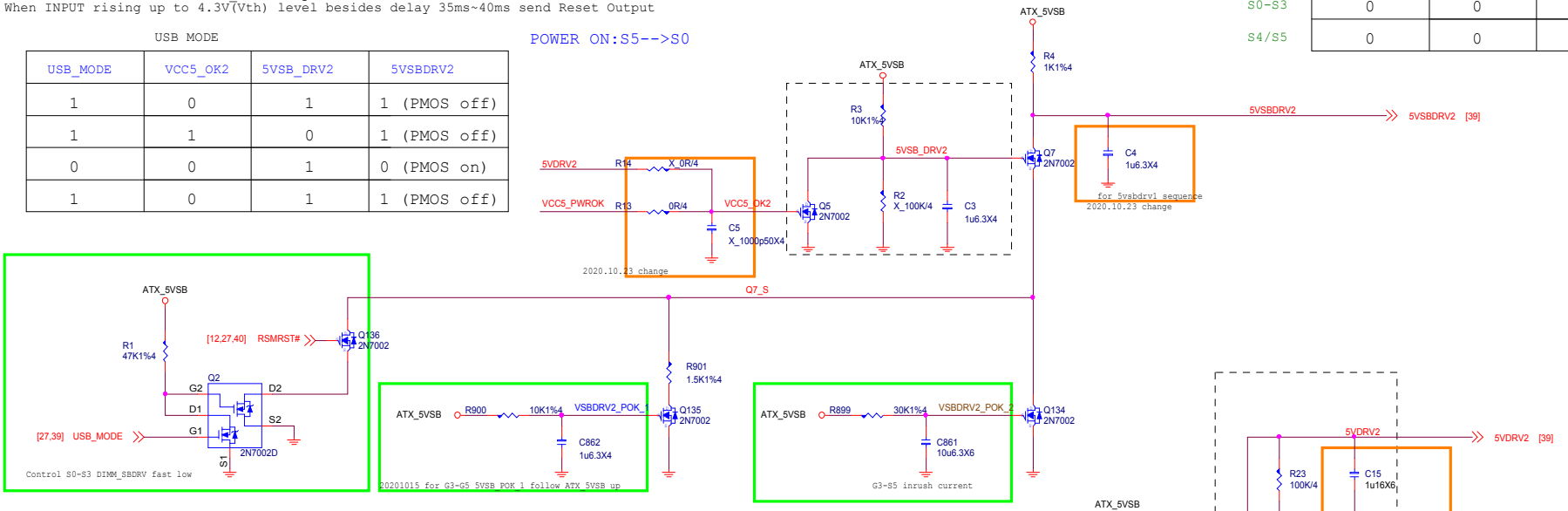
ENABLE RESUME BY USB DEVICE

	USB_MODE	VCC5_OK2	5VSB_DRV2	5VSBDRV2
G3-S5	0	0	1	0 (PMOS on)
S5-S0	0	1	0	1 (PMOS off)
S0-S3	0	0	1	0 (PMOS on)
S4/S5	0	0	1	0 (PMOS on)

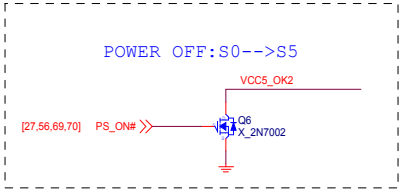
USB MODE

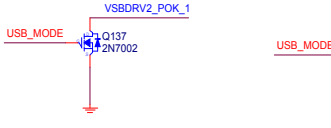
	USB_MODE	VCC5_OK2	5VSB_DRV2	5VSBDRV2
G3-S5	1	0	1	1 (PMOS off)
S5-S0	1	1	0	1 (PMOS off)
S0-S3	0	0	1	0 (PMOS on)
S4/S5	1	0	1	1 (PMOS off)

POWER ON:S5-->S0



POWER OFF:S0-->S5





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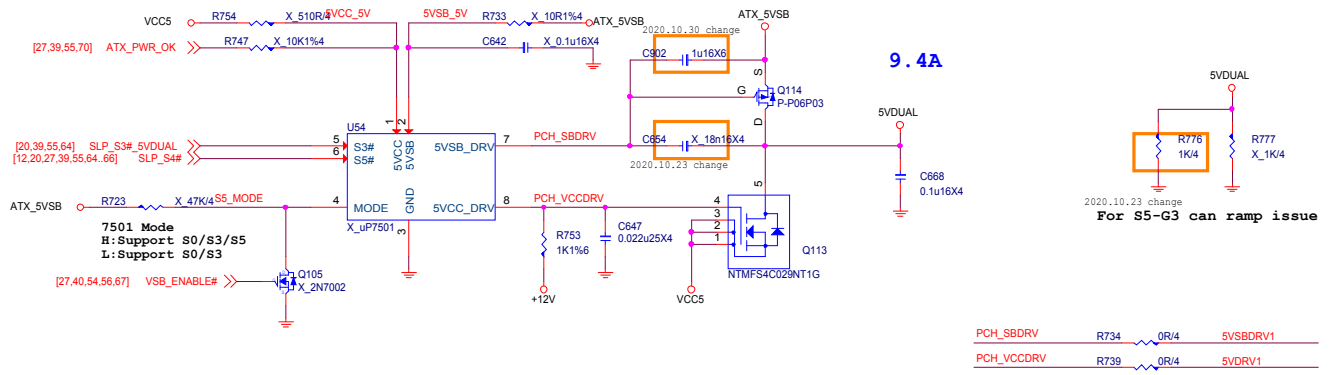
5VDUAL

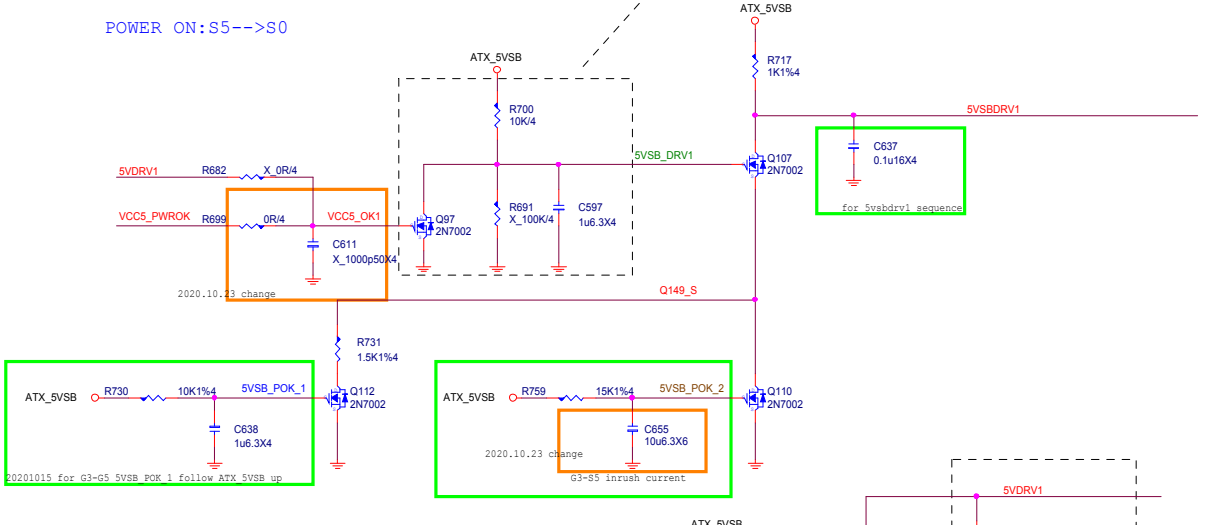


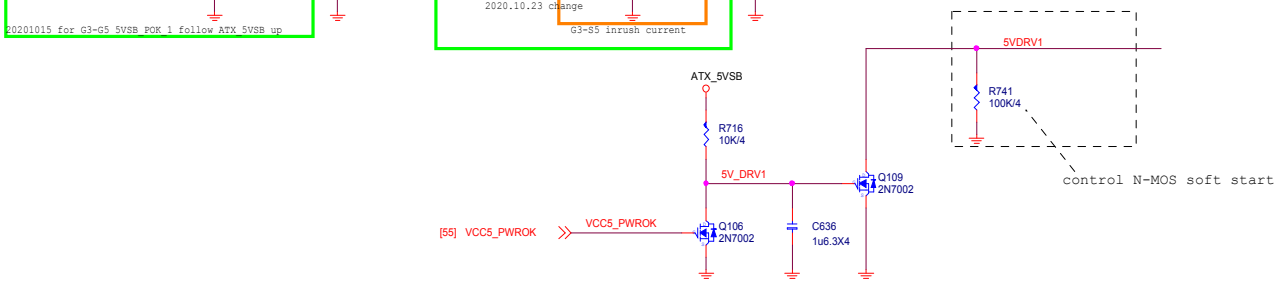
PCH_SBDRV R734 0R/4 5VSBDRV1

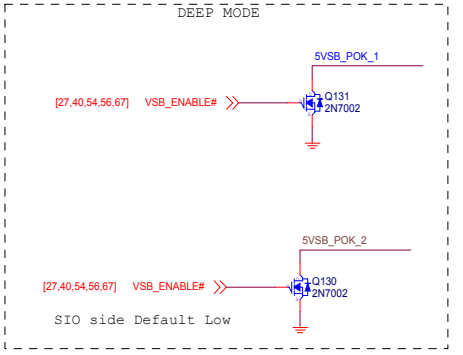
PCH_VCCDRV R739 0R/4 5VDRV1

control P-MOS soft start and waiting ATX_5VSB ramp to 100%

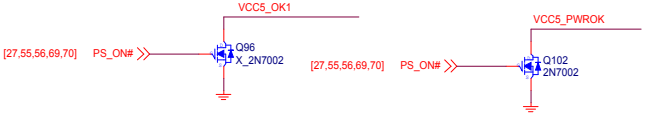
POWER ON:S5-->S0







POWER OFF:S0-->S5



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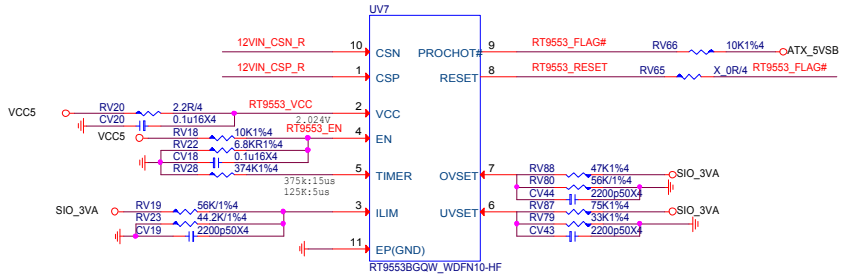
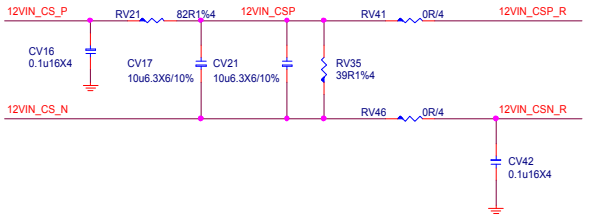
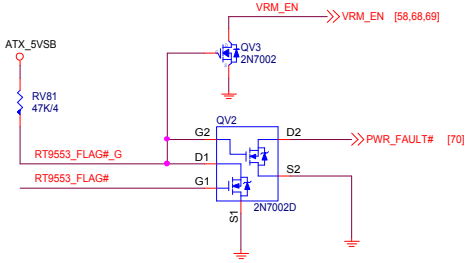
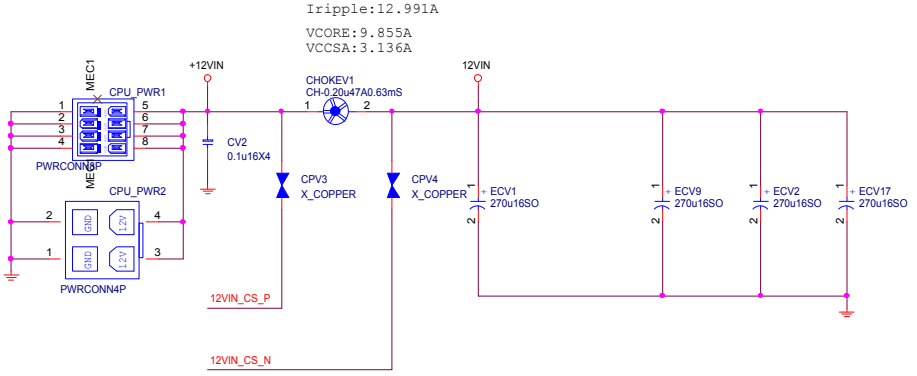
POWER METER

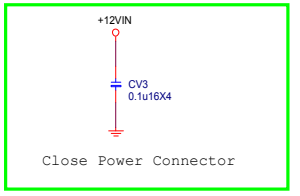
OCP: 45A for 8 core 193A support











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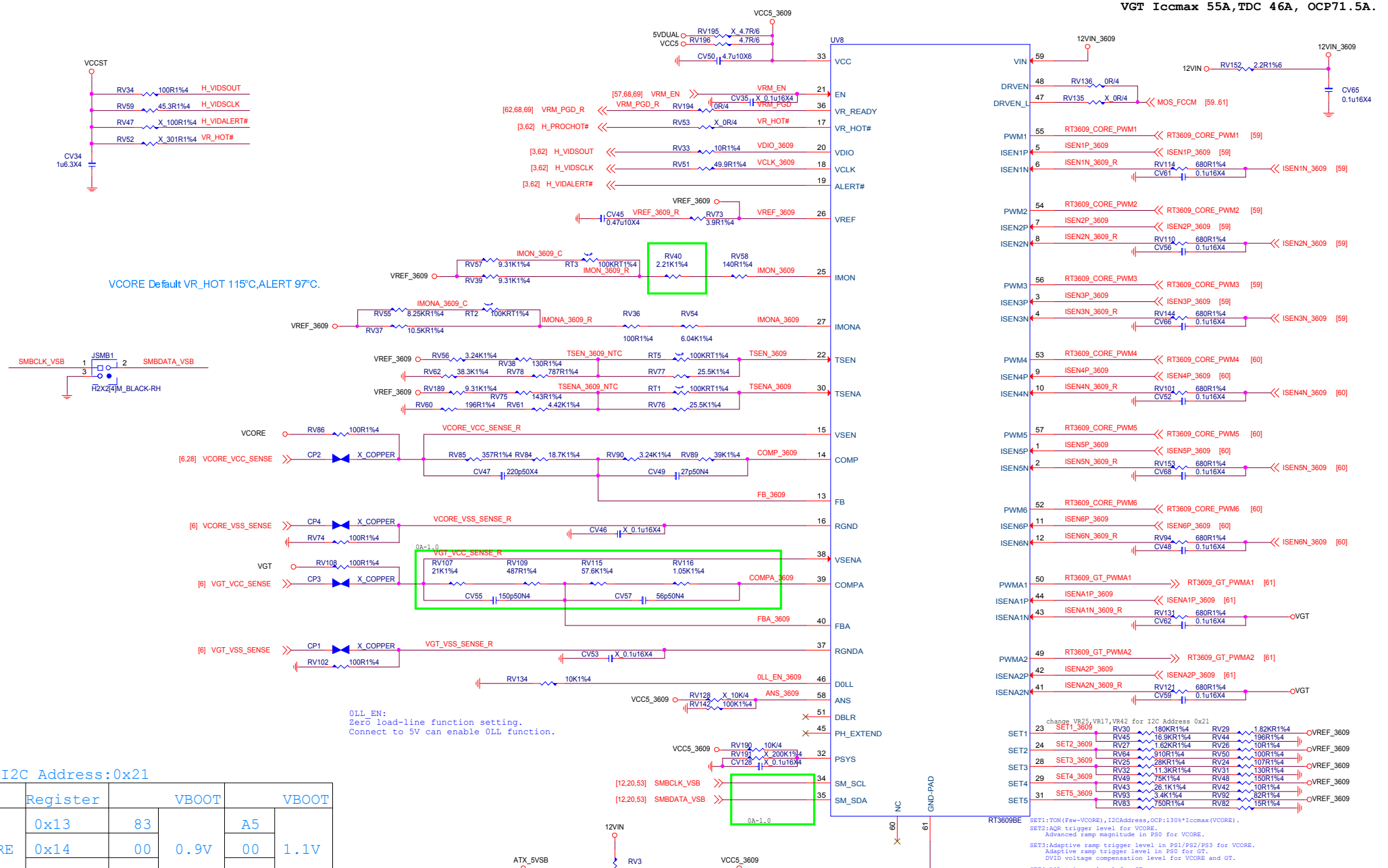
VCORE Iccmax 245A,TDC 175A, OCP318A.
VGT Iccmax 55A,TDC 46A, OCP71.5A.



I2C Address:0x21

	Register	VBOOT		VBOOT	
VCORE	0x13	83	0.9V	A5	1.1V
	0x14	00		00	
	0x12	01		01	
VGT	0x53	83	0.9V	A5	1.1V
	0x54	00		00	
	0x52	01		01	

Jumper insert,VCORE/VGT 0.9V.

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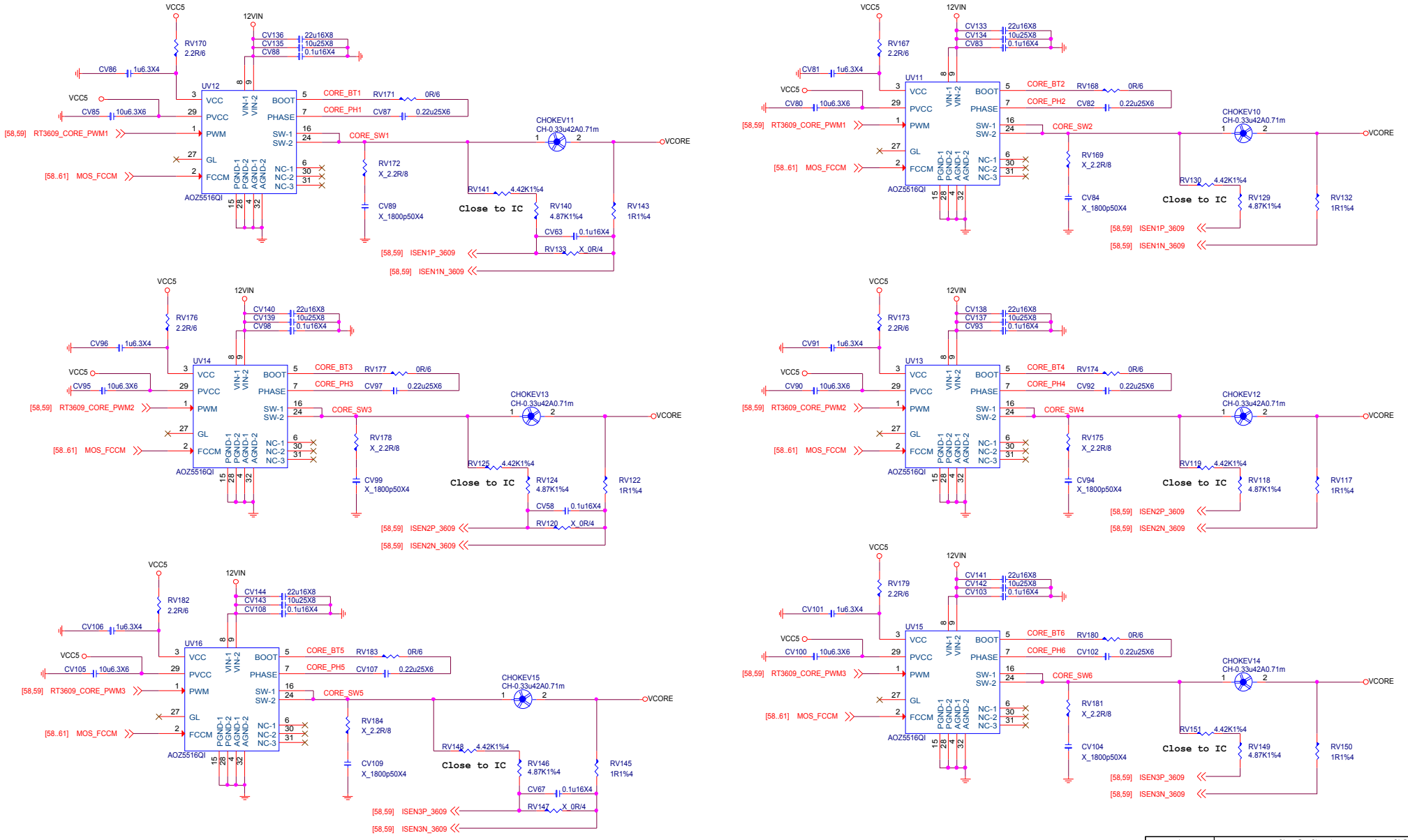

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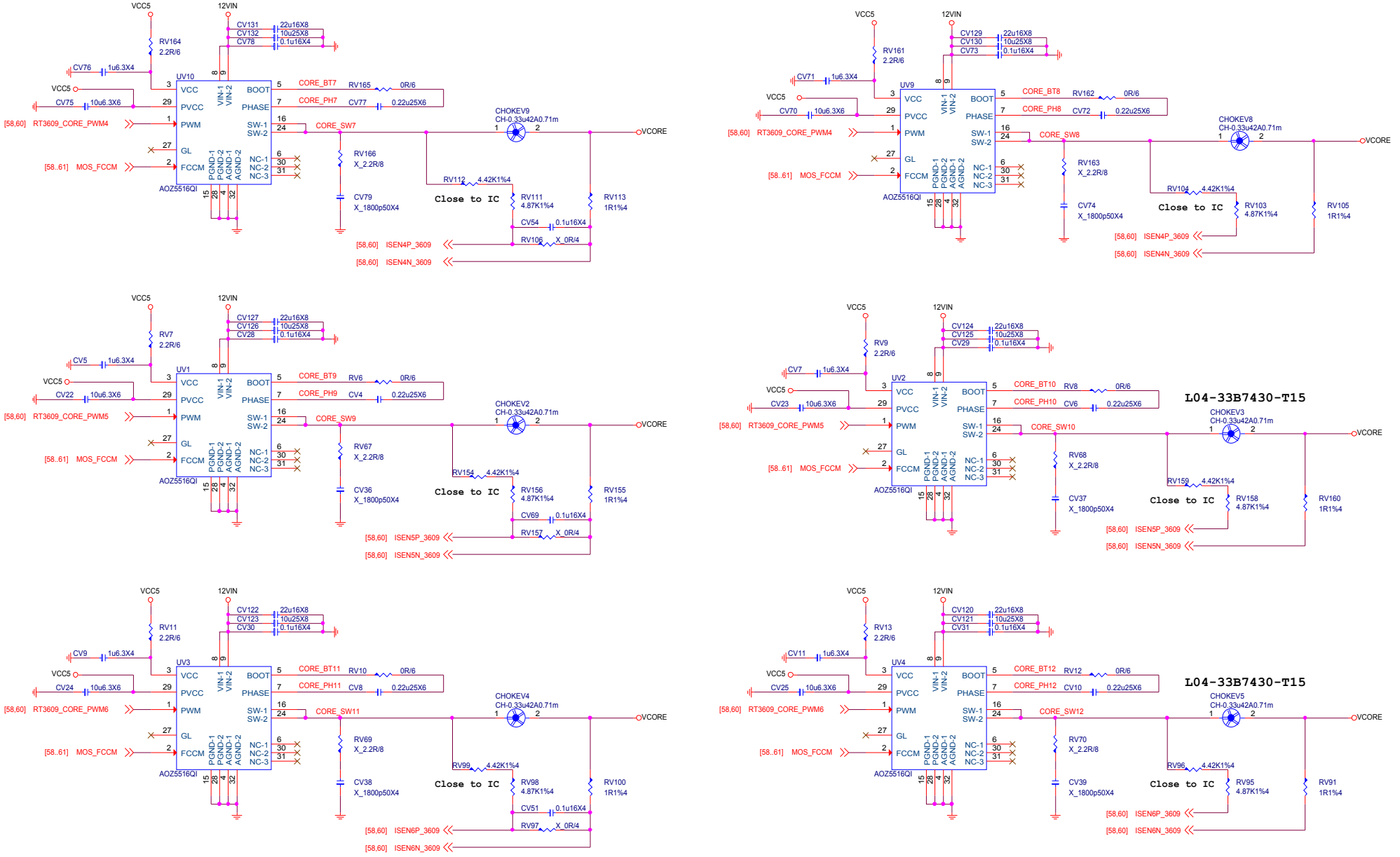

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D09	
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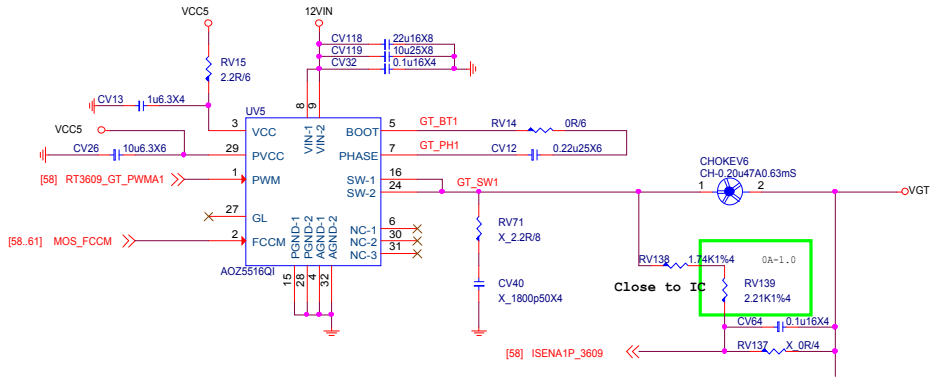

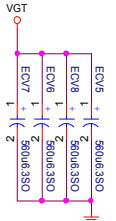

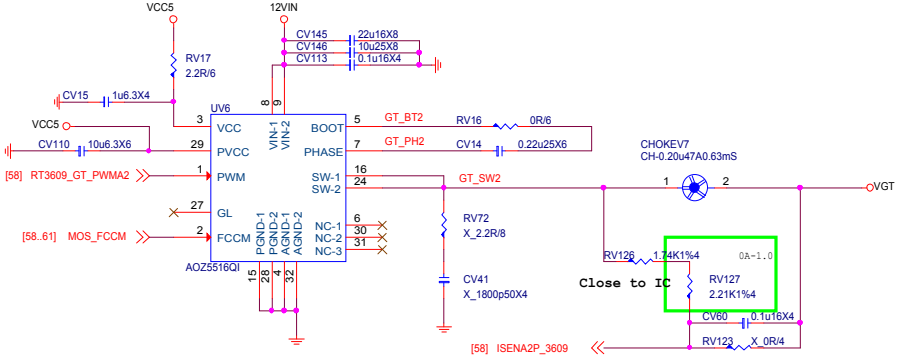

MICRO-STAR INT'L CO.,LTD		
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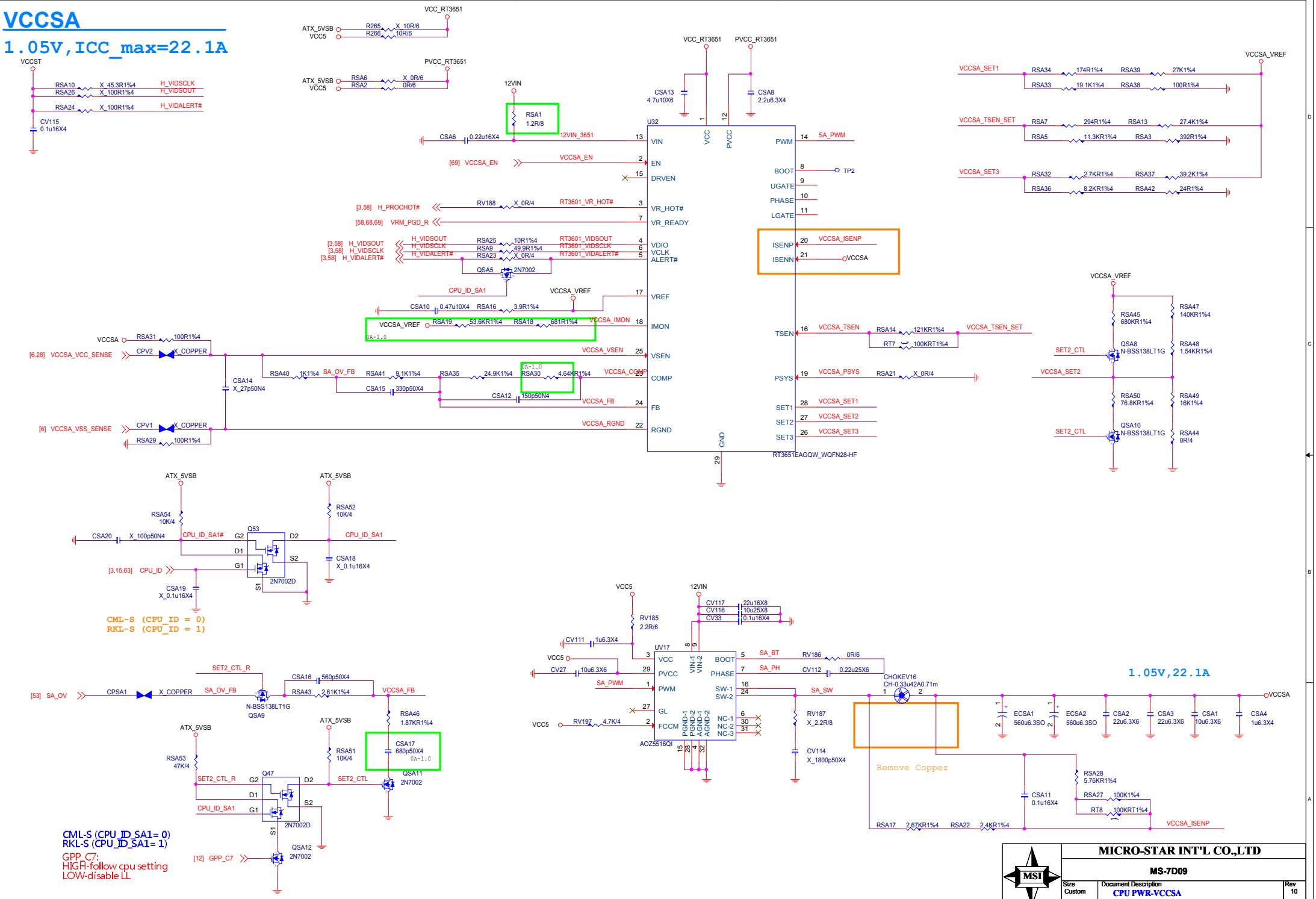
VCCSA

1.05V,ICC_max=22.1A



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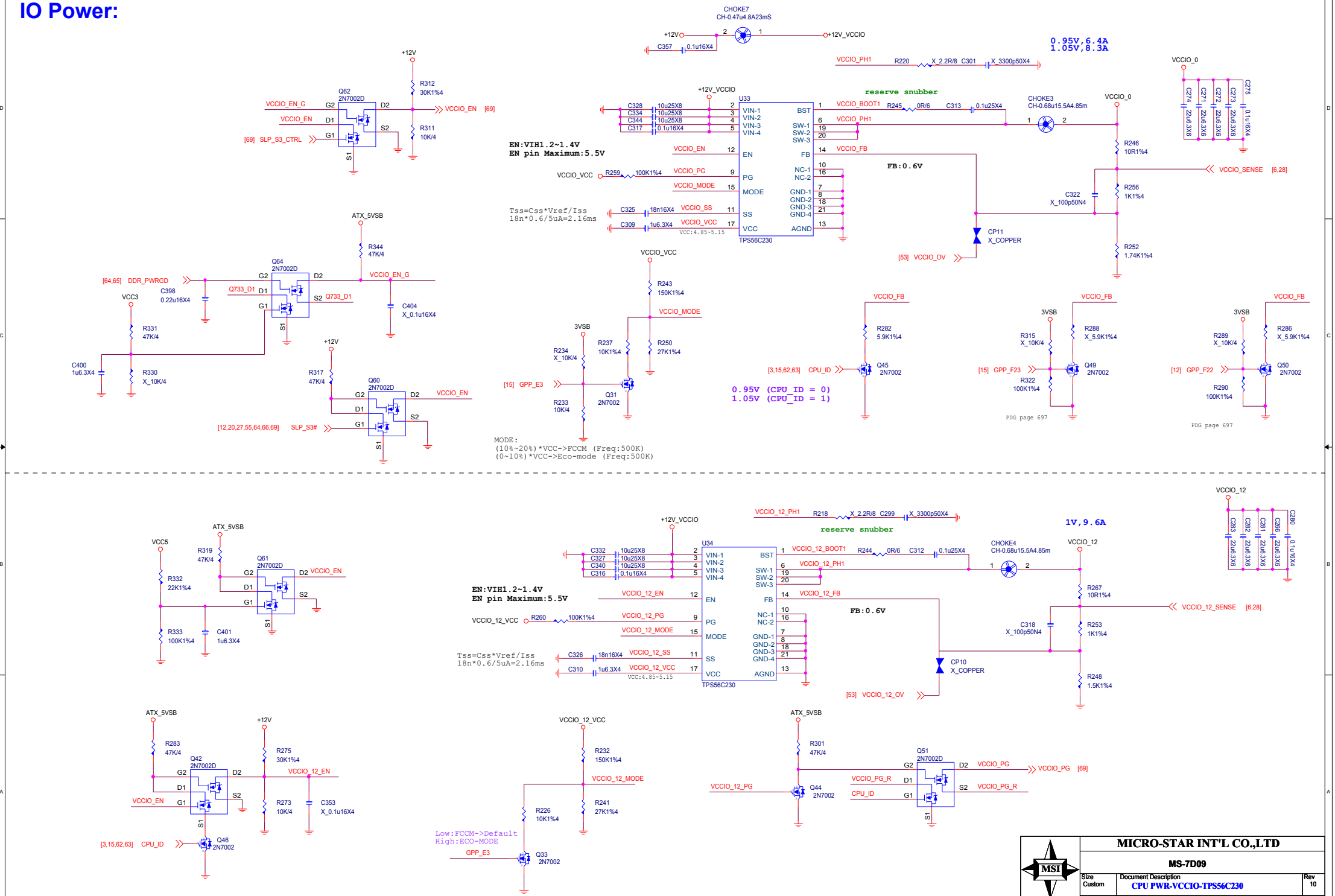
IO Power:


CHOKE7
CH-0.47u4.8A23mS
+12V
+12V_VCCIO
C357 0.1u16X4
0.95V,6.4A
1.05V,8.3A
VCCIO_PH1 R220 X_2.2R/8 C301 X_3300p50X4
reserve snubber
VCCIO_BOOT1 R245 0R/6 C313 0.1u25X4
CHOKE3
CH-0.68u15.5A4.85m
VCCIO_0
C274 C271 C272 C273 C275
22u6.3X6 22u6.3X6 22u6.3X6 22u6.3X6 0.1u16X4
Q62
2N7002D
VCCIO_EN_G
VCCIO_EN
[69] SLP_S3_CTRL
R312
30K1%4
R311
10K4
VCCIO_EN [69]
C328 C334 C344 C317
10u25X8 10u25X8 10u25X8 0.1u16X4
U33
VIN-1 VIN-2 VIN-3 VIN-4
BST SW-1 SW-2 SW-3
EN
FB
PG
MODE
SS
VCC
NC-1 NC-2
GND-1 GND-2 GND-3 GND-4
AGND
TPS56C230
EN:VIH1.2~1.4V
EN pin Maximum:5.5V
VCCIO_EN
VCCIO_PG
VCCIO_MODE
VCCIO_SS
VCCIO_VCC
VCCIO_FB
FB:0.6V
VCCIO_VCC R259 100K1%4
Tss=Css*Vref/Iss
18n*0.6/5uA=2.16ms
C325 18n16X4
C309 1u6.3X4
VCC:4.85~5.15
R246
10R1%4
R256
1K1%4
R252
1.74K1%4
C322
X_100p50N4
CP11
X_COPPER
[53] VCCIO_OV
VCCIO_SENSE [6,28]
ATX_5VSB
R344
47K/4
Q64
2N7002D
[64,65] DDR_PWRGD
C398
0.22u16X4
Q733_D1
VCCIO_EN_G
C404
X_0.1u16X4
VCC3
R331
47K/4
C400
1u6.3X4
R330
X_10K/4
+12V
R317
47K/4
Q60
2N7002D
VCCIO_EN
[12,20,27,55,64,66,69] SLP_S3#
VCCIO_VCC
R243
150K1%4
VCCIO_MODE
3VSB
R234
X_10K/4
R237
10K1%4
R250
27K1%4
[15] GPP_E3
Q31
2N7002
R233
10K/4
MODE:
(10%~20%)*VCC->FCCM (Freq:500K)
(0~10%)*VCC->Eco-mode (Freq:500K)
VCCIO_FB
R282
5.9K1%4
[3,15,62,63] CPU_ID
Q45
2N7002
0.95V (CPU_ID = 0)
1.05V (CPU_ID = 1)
3VSB
R315
X_10K/4
R288
X_5.9K1%4
[15] GPP_F23
Q49
2N7002
R322
100K1%4
PDG page 697
R289
X_10K/4
R286
X_5.9K1%4
[12] GPP_F22
Q50
2N7002
R290
100K1%4
PDG page 697
VCCIO_12
C283 C282 C281 C286 C280
22u6.3X6 22u6.3X6 22u6.3X6 22u6.3X6 0.1u16X4
VCCIO_12_PH1 R218 X_2.2R/8 C299 X_3300p50X4
reserve snubber
1V,9.6A
VCCIO_12_BOOT1 R244 0R/6 C312 0.1u25X4
CHOKE4
CH-0.68u15.5A4.85m
VCCIO_12
VCC5
R319
47K/4
Q61
2N7002D
VCCIO_EN
R332
22K1%4
R333
100K1%4
C401
1u6.3X4
C332 C327 C340 C316
10u25X8 10u25X8 10u25X8 0.1u16X4
U34
TPS56C230
EN:VIH1.2~1.4V
EN pin Maximum:5.5V
VCCIO_12_EN
VCCIO_12_PG
VCCIO_12_MODE
VCCIO_12_SS
VCCIO_12_VCC
VCCIO_12_FB
FB:0.6V
VCCIO_12_VCC R260 100K1%4
Tss=Css*Vref/Iss
18n*0.6/5uA=2.16ms
C326 18n16X4
C310 1u6.3X4
VCC:4.85~5.15
R267
10R1%4
R253
1K1%4
R248
1.5K1%4
C318
X_100p50N4
CP10
X_COPPER
[53] VCCIO_12_OV
VCCIO_12_SENSE [6,28]
R283
47K/4
Q42
2N7002D
R275
30K1%4
VCCIO_12_EN
R273
10K/4
C353
X_0.1u16X4
[3,15,62,63] CPU_ID
Q46
2N7002
R232
150K1%4
VCCIO_12_MODE
R226
10K1%4
R241
27K1%4
Low:FCCM->Default
High:ECO-MODE
GPP_E3
Q33
2N7002
R301
47K/4
Q51
2N7002D
VCCIO_PG
VCCIO_PG [69]
VCCIO_12_PG
Q44
2N7002
VCCIO_PG_R
CPU_ID
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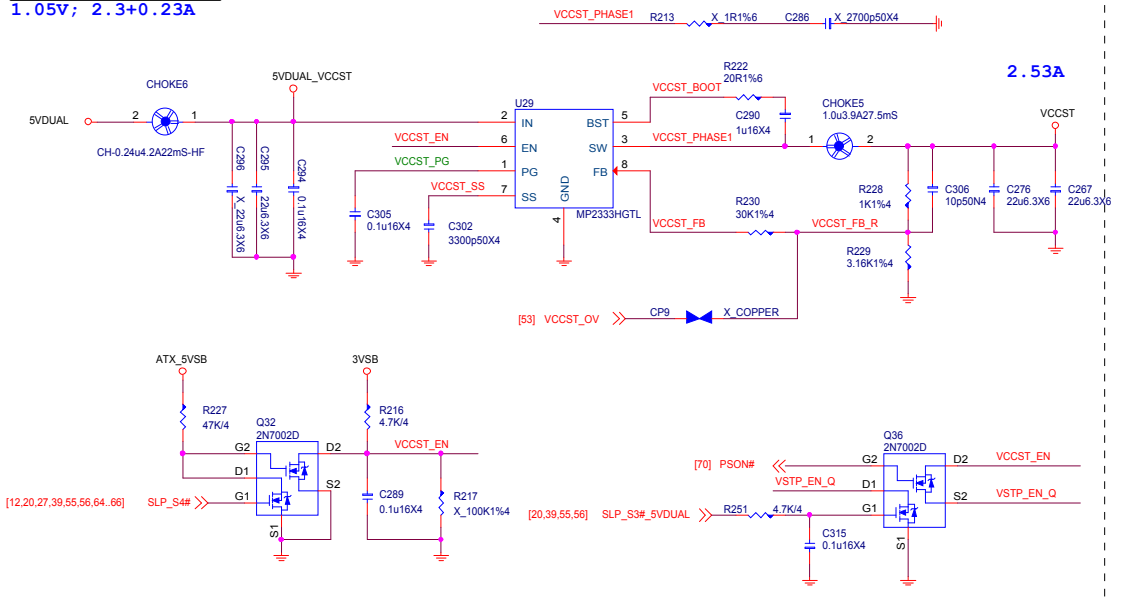
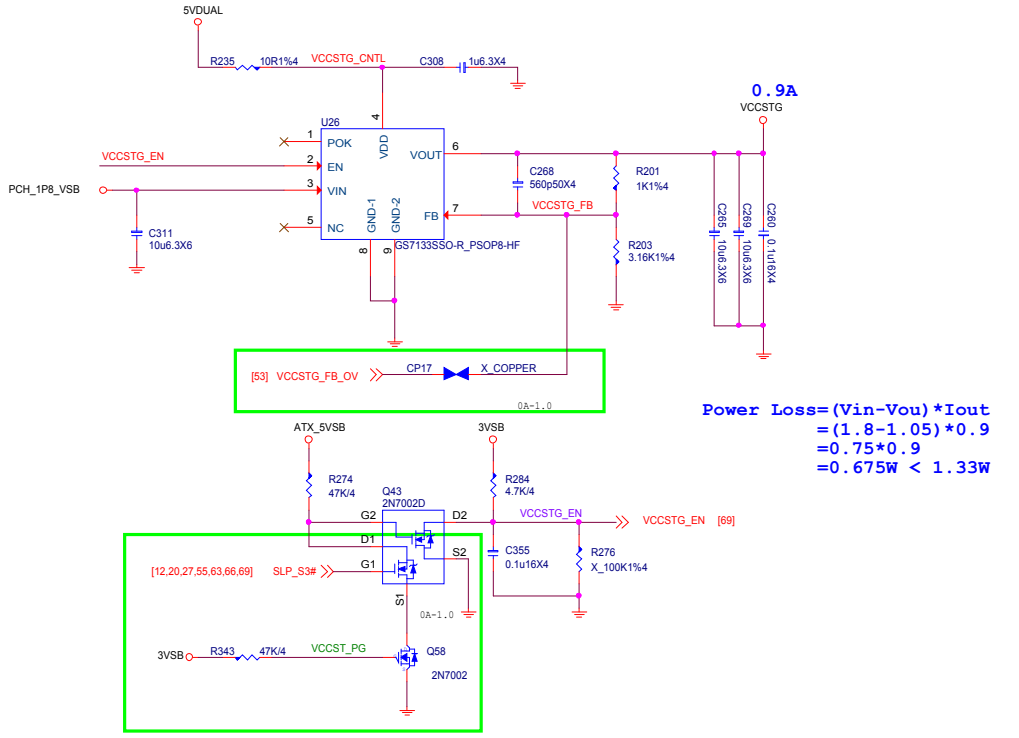
VCCST

1.05V; 2.3+0.23A



VCCSTG

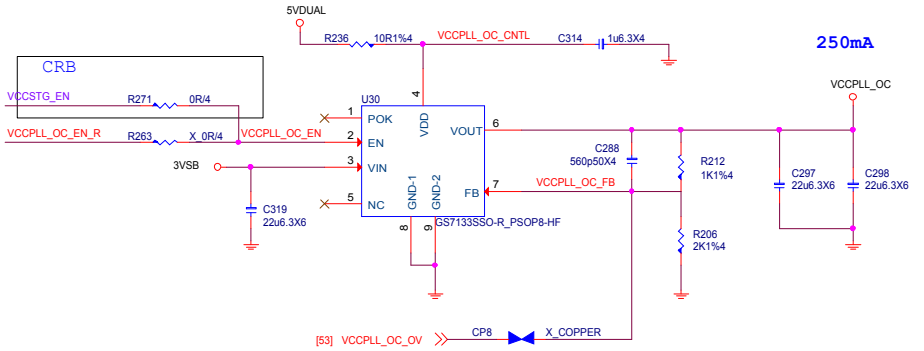
1.05V; 0.9A



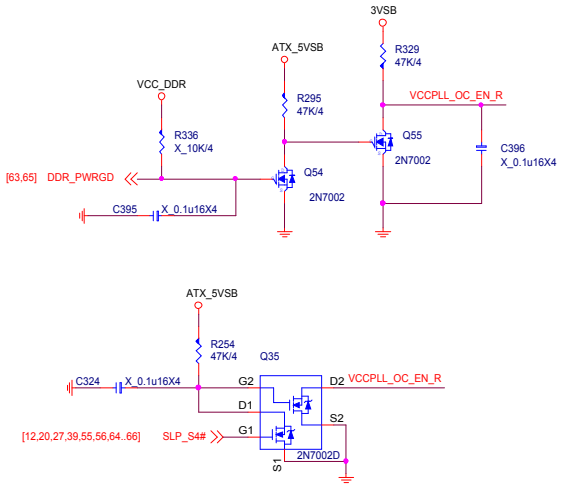
Power Loss=(Vin-Vou)*Iout
=(1.8-1.05)*0.9
=0.75*0.9
=0.675W < 1.33W

VCCPLL_OC

1.2V; 250mA



Power Loss=(Vin-Vou)*Iout
=(3.3-1.2)*0.25
=2.1*0.25
=0.53W < 1.33W



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DDR4 Power:1.2V,14.4A *OCP:18A*

Rocset = 1.2 * Imax * Rdson(low) / Iocset
= 21.6* 4mohm / 10uA
= 8.64K

4.3A FOR CPU

9.1A FOR 4DIMM

0.7A FOR DDR VTT

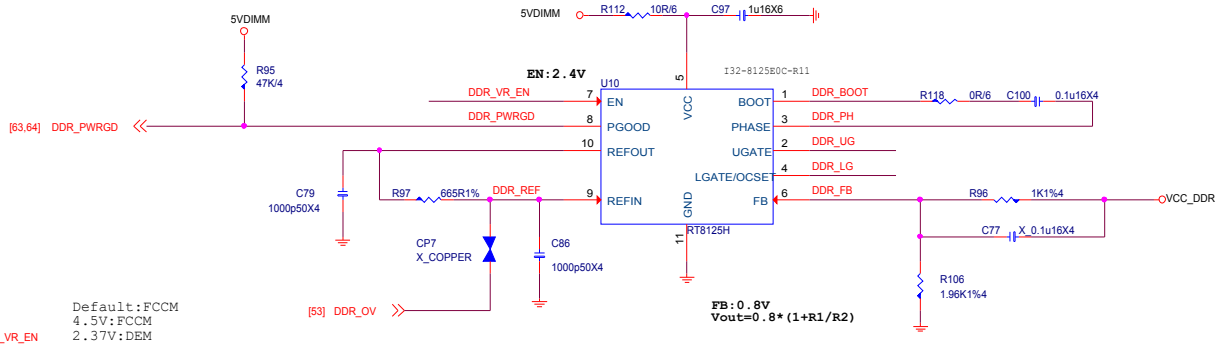
Iocp =Rocset* Iocset /Rdson(low)
=7.15K*10uA/3.3m
=21.66A

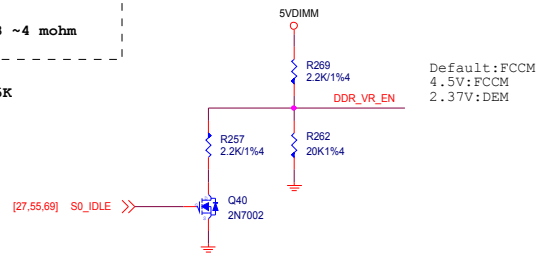
Iocp =Rocset* Iocset /Rdson(max)
=7.15K*10uA/4m
=17.88A

Rocset = 1.2 * Imax * Rdson(low) / Iocset
= 21.6* 3.3mohm / 10uA
= 7.12K

Rdson(Low Side) 5V
D03-4C02403-005:3.3 ~4 mohm

Note: Rocset(min)=5K

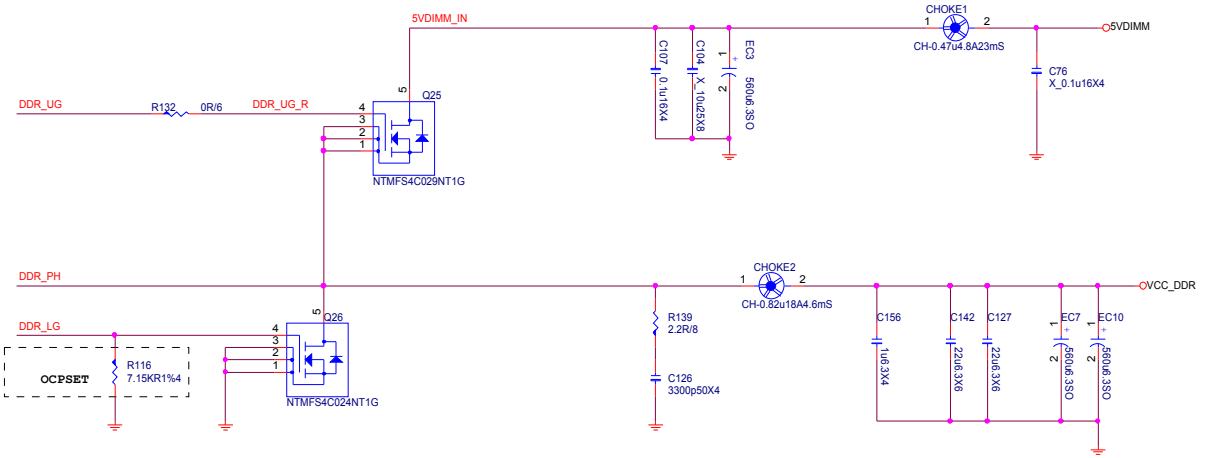


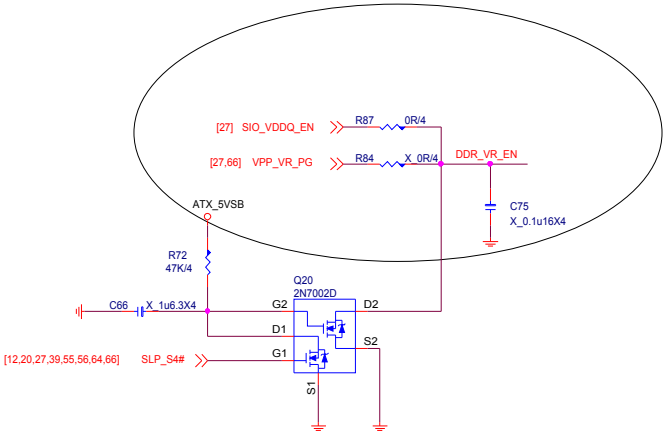


Default:FCCM
4.5V:FCCM
2.37V:DEM

Default:FCCM
L:FCCM
H:DEM

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 14.4 * 0.43
= 6.192A





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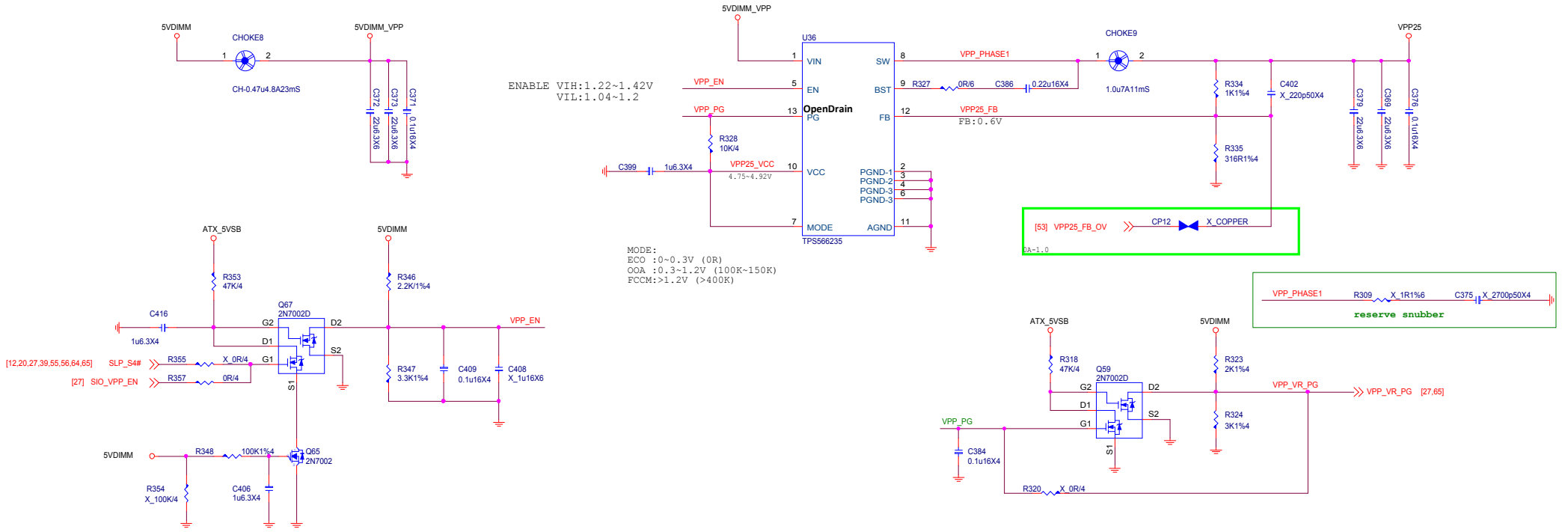
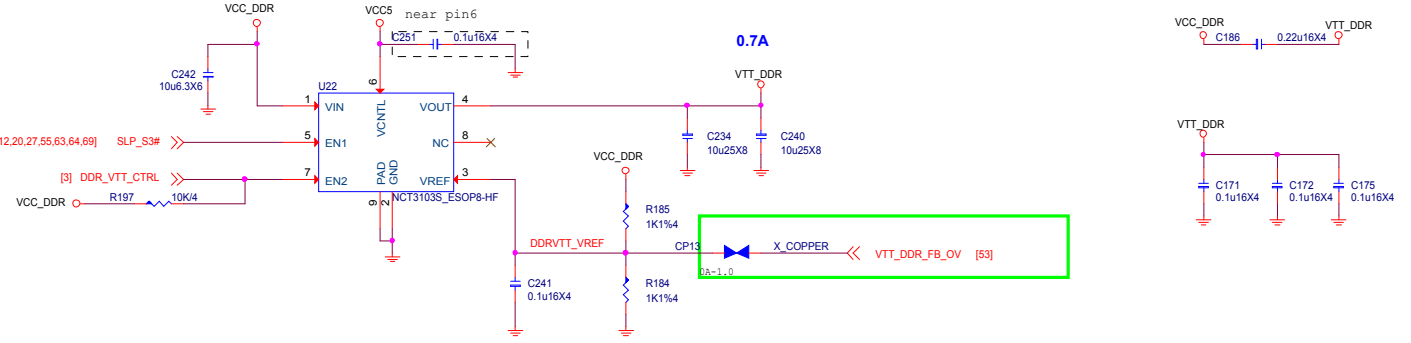
VPP25 Power:2.5V,6A(For DIMM LED)



DDR VTT Power



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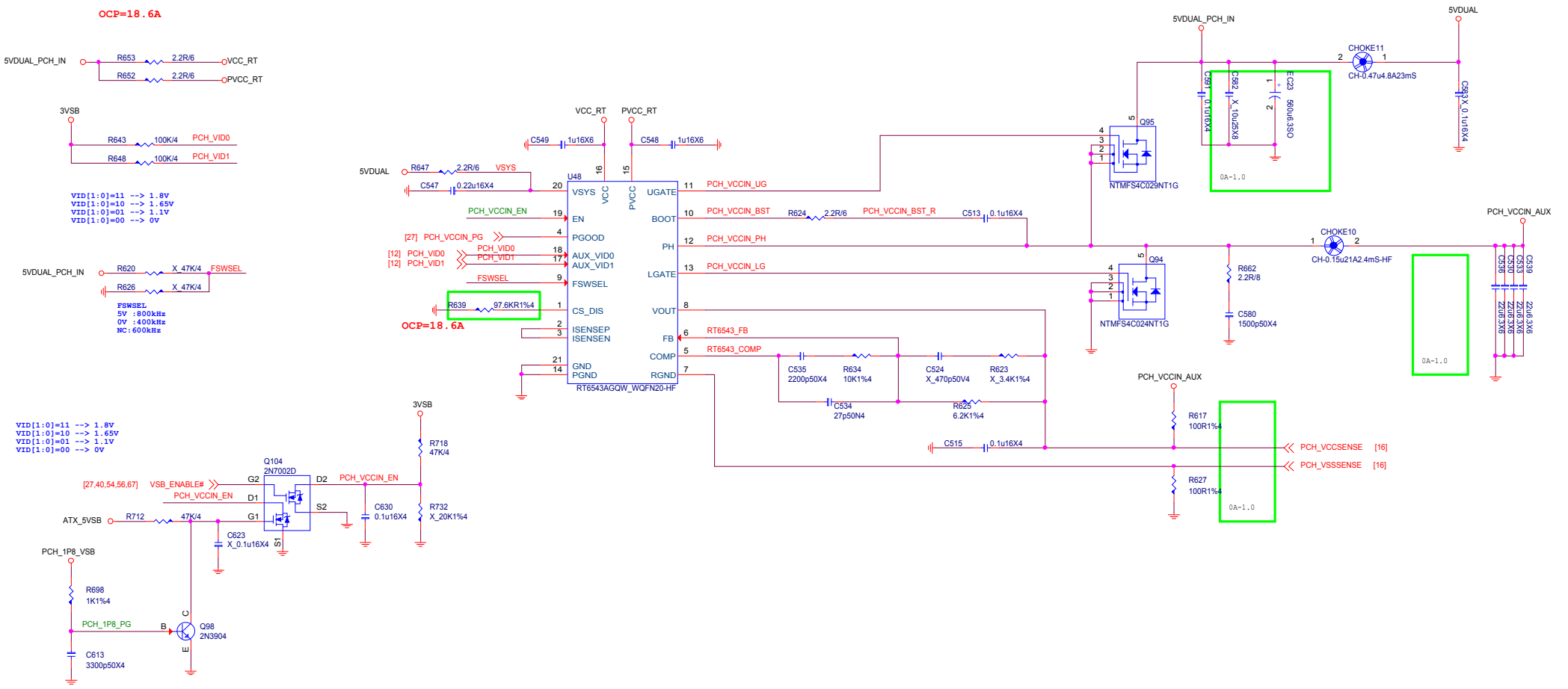
PCH_Power:VCCIN_AUX

1.8V 11.2A

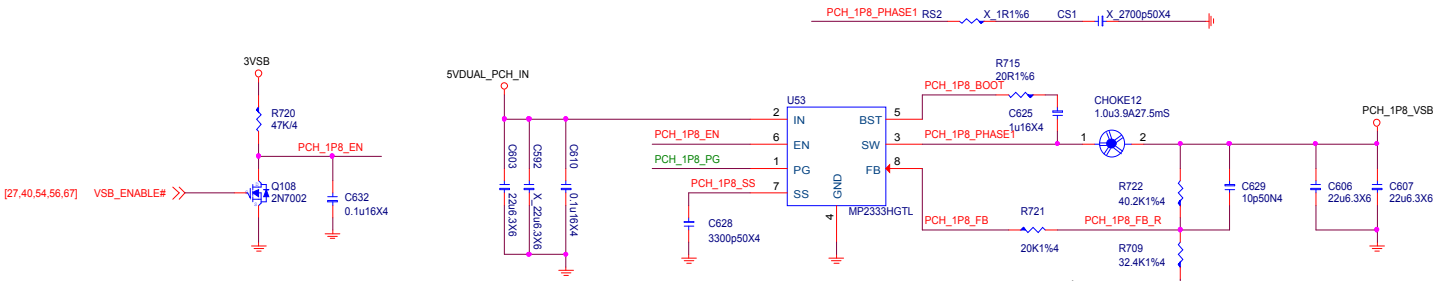
OCP=18.6A

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 11.2 * 0.43
     = 4.22A
```



PCH_1P8_VSB

1.8V; 2.048A




```
Vout = Vref * (1 + R1606/R1607)
     = 0.8 * (1 + 40.2K/32.4K)
     = 0.8 * 2.241
     = 1.793V
```

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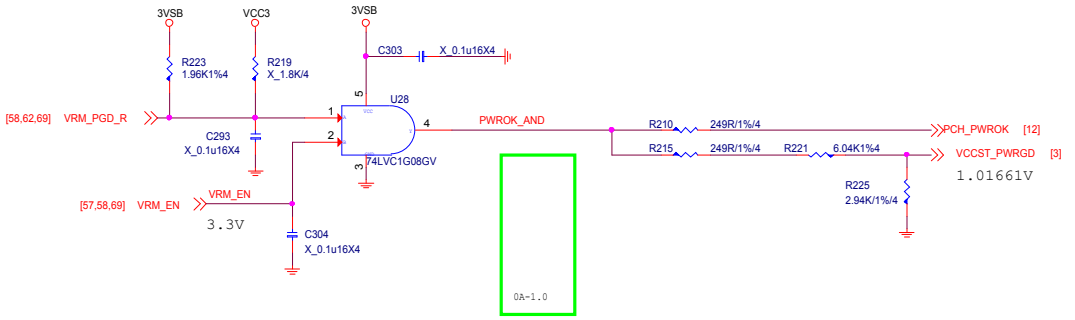
PCH_PWROK/VCCST_PWRGD



0A-1.0

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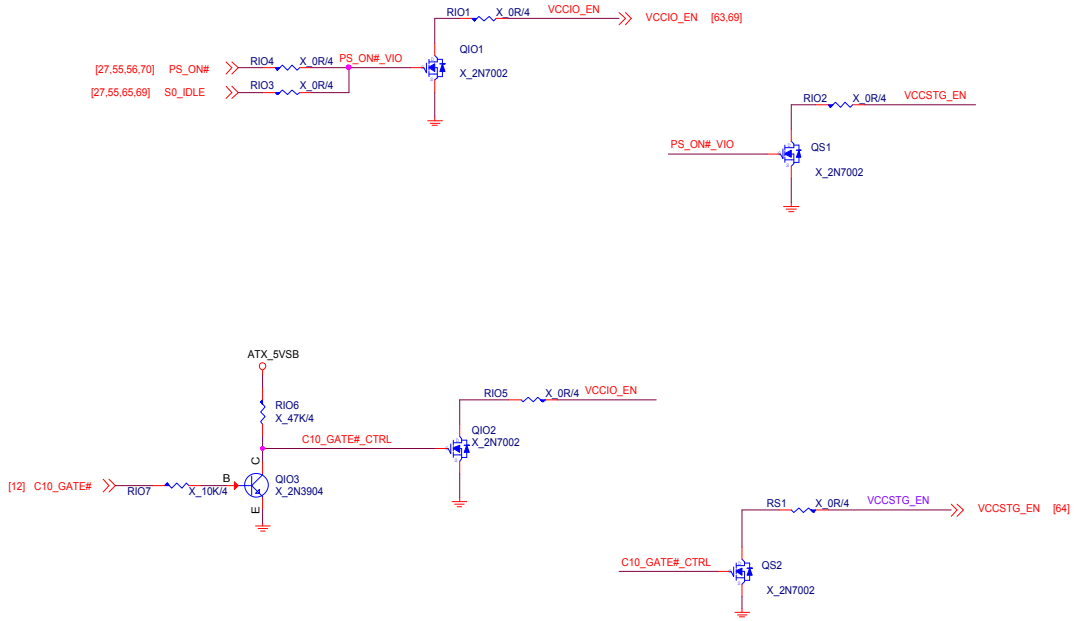
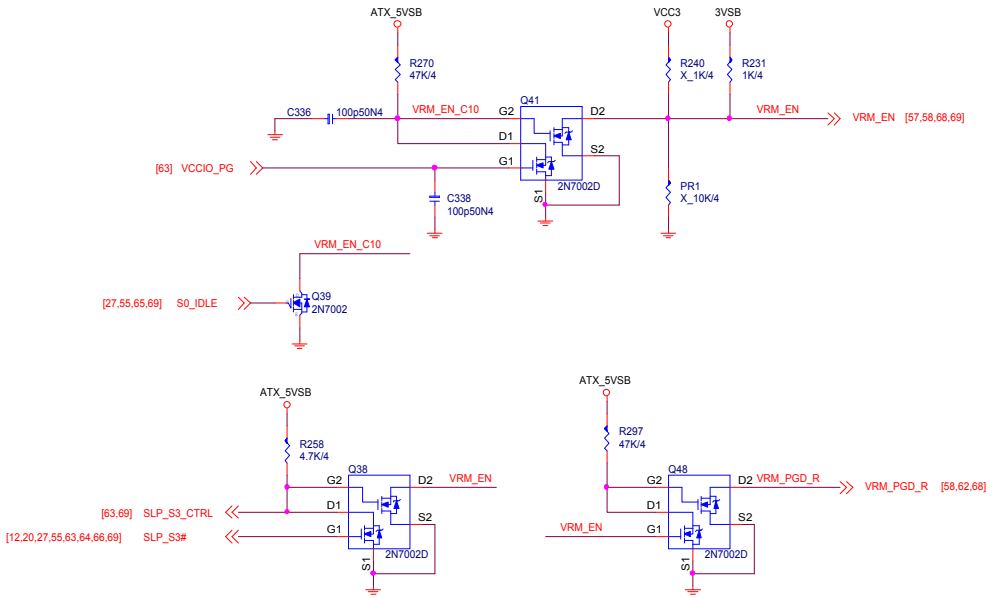
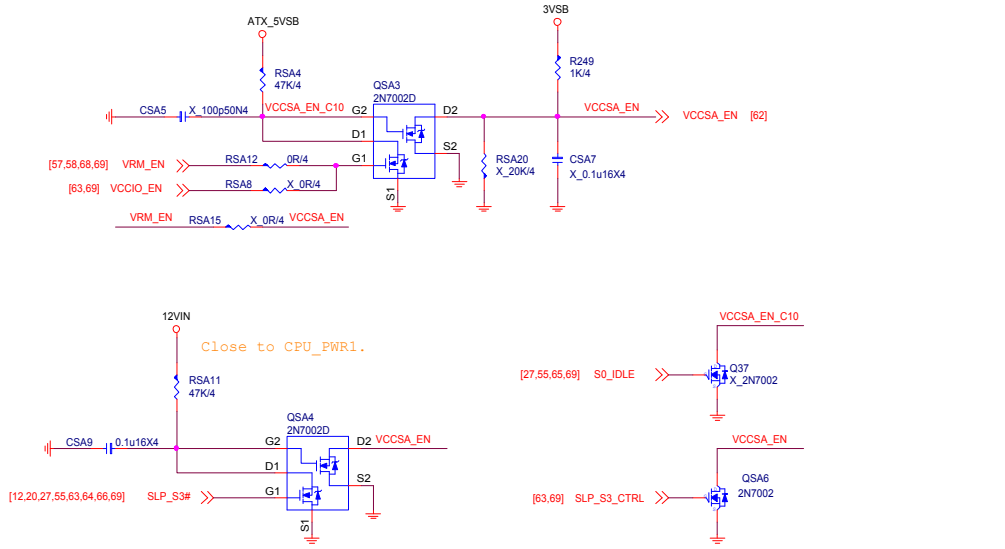
S0IX: VCCIO/VCCSTG OFF



PWR-VRM-Seqence



PWR-VCCSA-Seqence



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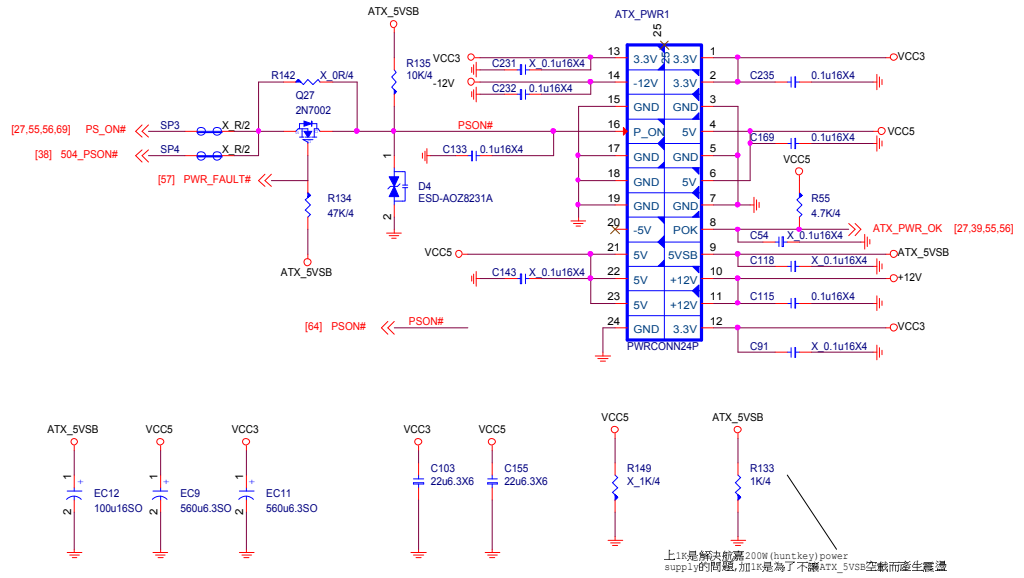
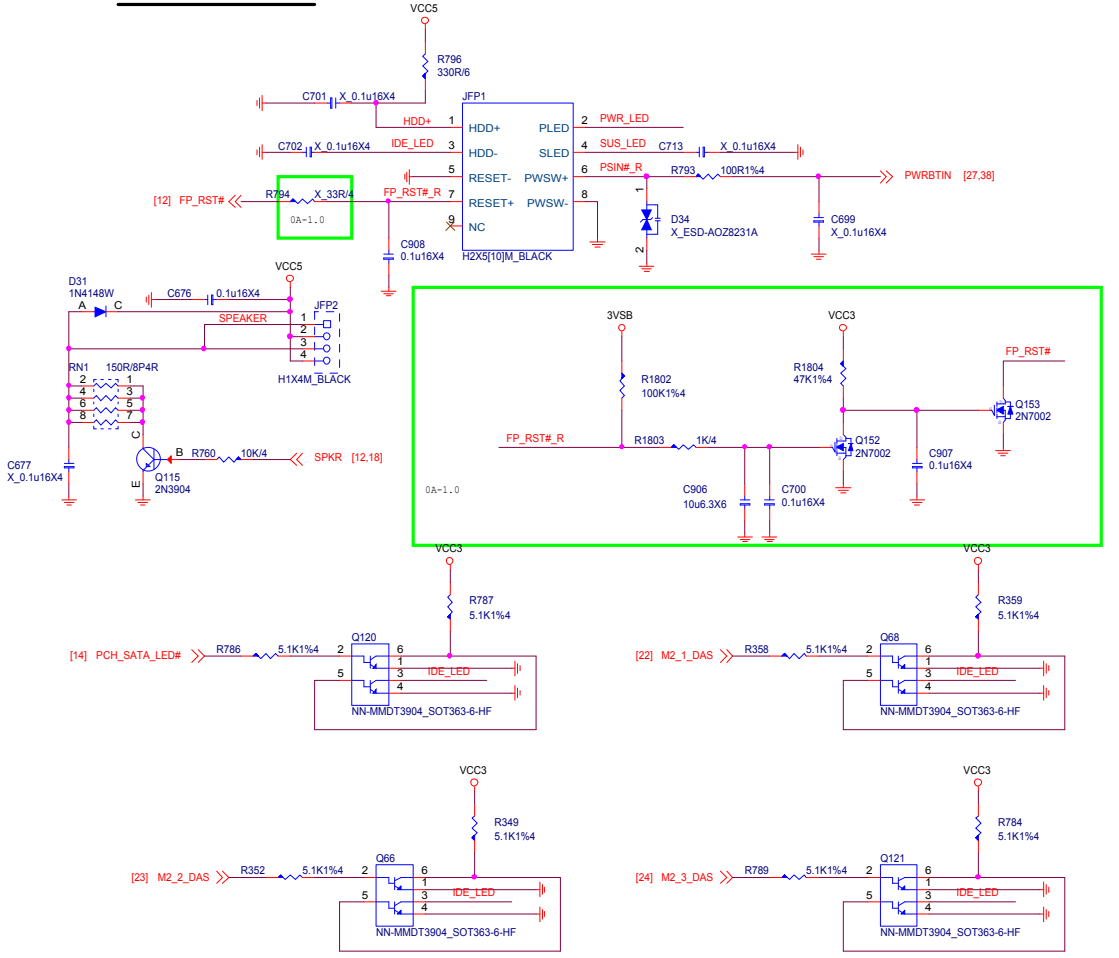
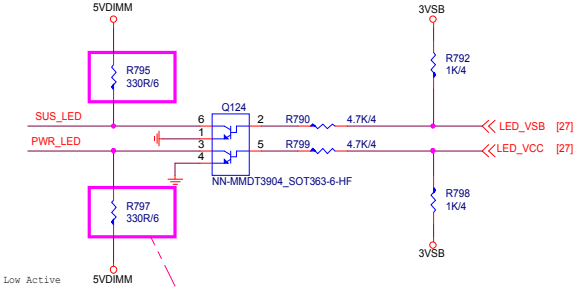
ATX POWER CONNECTOR



FRONT PANNEL



Front Panel LED



Reserve pull high to 5VDIMM if PM don't want PLED light in deep mode.

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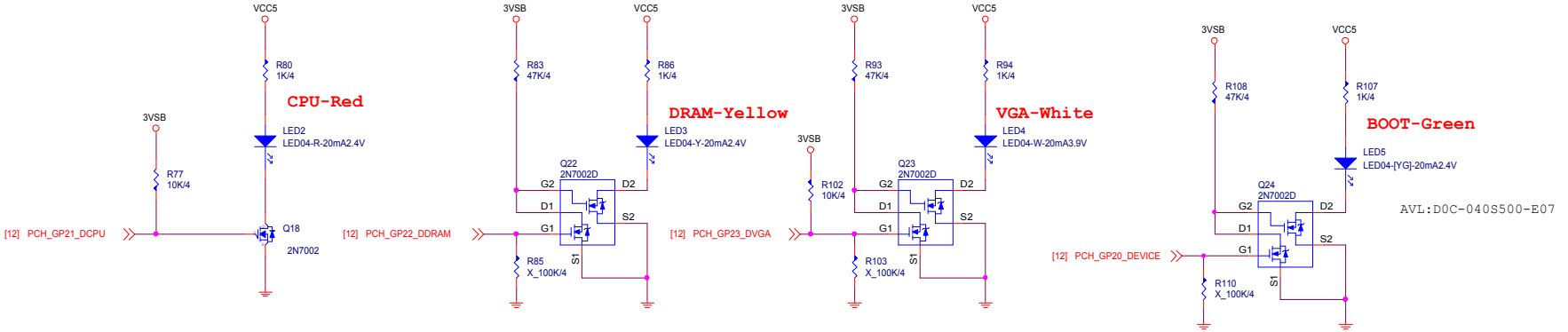
EZ Debug LED



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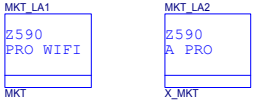
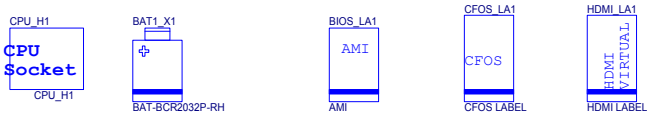
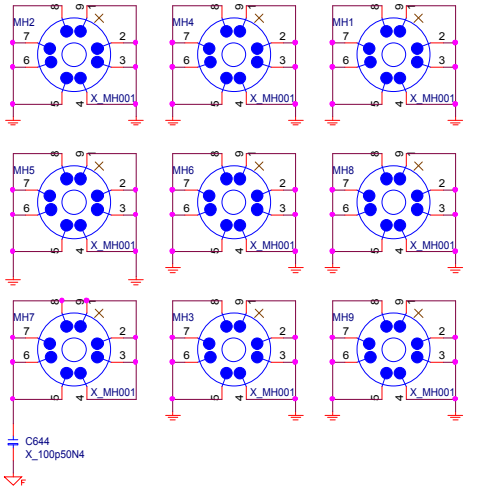
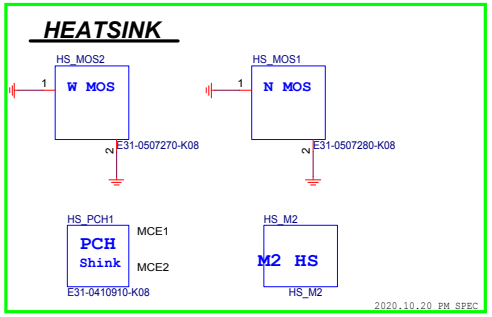




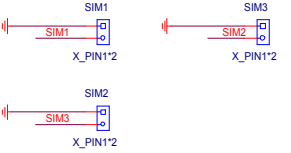
Mounting Holes



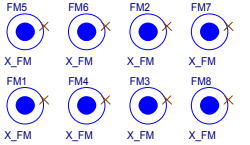
HEATSINK



Simulation



Optical Fiducial Marks-120



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